

EXHIBIT 2

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

| | | |
|---------------------------|---|---------------------------|
| POWER INTEGRATIONS, INC., | : | |
| a Delaware corporation | : | |
| | : | |
| Plaintiff, | : | Case No.: 20-cv-00015-CFC |
| | : | |
| v. | : | |
| | : | |
| COGNIPOWER LLC, | : | JURY TRIAL REQUESTED |
| | : | |
| Defendant. | : | |

COGNIPOWER LLC’S INVALIDITY CONTENTIONS

In compliance with paragraph 5 of the proposed scheduling order (D.I. 25-1), CogniPower LLC provides its Invalidity Contentions to Power Integrations, Inc. The Invalidity Contentions are for the asserted claims of U.S. Patent Nos. 9,374,011 (“the ’011 Patent”) and 9,166,486 (“the ’486 Patent”) (collectively “the Asserted Patents”). Power Integrations currently asserts claims 1, 8, 9, and 17 of the ’011 Patent and claims 1-3, 5-9, 11, 13, 16-18, 20-23, and 25-26 of the ’486 Patent. CogniPower reserves the right to supplement or modify these invalidity contentions as the case progresses consistent with the Federal Rules, the Local Rules, and the Court’s scheduling order.

CogniPower uses the application dates of the Asserted Patents as the priority date for these contentions. Power Integrations admits that the Asserted Patents do not claim priority to any earlier applications. CogniPower reserves the right to

amend its invalidity contentions, as necessary, should Power Integrations show that any asserted claims of the Asserted Patents are entitled to an earlier priority date.

I. INVALIDITY CONTENTIONS

a. Prior Art

Under paragraph 5(a) of the proposed scheduling order, CogniPower identifies the following prior art that invalidates the asserted claims of the asserted patents. CogniPower reserves the right to rely on the earliest publication or priority dates to which each of the prior art references are entitled, including dates on which a claim of priority may be based for patent references that are any of a divisional, continuation, or continuation-in-part of an earlier filed patent application.

| Patent Number | Country of Origin | Date Issued | Bates Number |
|--|--------------------------|--------------------|-----------------------------------|
| U.S. Pat. No. 9,071,152 (Morong) | U.S. | 2015-06-30 | PI_COGNI000001- PI_COGNI000012 |
| U.S. Pat. No. 7,385,832 (Allinder) | U.S. | 2008-06-10 | PI_COGNI000013- PI_COGNI000021 |
| U.S. Pat. No. 7,746,050 (Djenguerian) | U.S. | 2010-06-29 | PI_COGNI000022- PI_COGNI000037 |

The prior art references identified above and cited in the attached claim charts may disclose the limitations of claims either explicitly or inherently. All of these references qualify as prior art to the asserted patents.

Morong (and the invention(s) embodied therein) qualify as prior art under at least 35 U.S.C. §§ 102(e) and 102(g). Morong claims priority to, and incorporates in full, two provisional applications: U.S. provisional application Nos. 61/667,473,

filed on July 3, 2012, and 61/727,795, filed on November 19, 2012. Both dates precede the effective filing dates of the Asserted Patents. CogniPower inventors William H. Morong and Thomas E. Lawson conceived of the invention(s) embodied in Morong at least as early as November 19, 2012, and they did not abandon, suppress, or conceal it. The invention(s) embodied in Morong is also embodied in the Accused Instrumentality as explained in CogniPower's Answer and incorporated herein. D.I. 19. Both Mr. Morong and Mr. Lawson have personal knowledge of the conception and development of the invalidating invention embodied in Morong and in the Accused Instrumentality.

Allinder qualifies as prior art under at least 35 U.S.C. § 102(b). Allinder is a printed publication published more than one year before both Asserted Patents' effective filing dates.

Djenguerian qualifies as prior art under at least 35 U.S.C. § 102(b). Djenguerian is a printed publication published more than one year before both Asserted Patents' effective filing dates.

b. Asserted Patents are Invalid Under 35 U.S.C. § 103

Morong combined with Allinder renders obvious claims 1, 8, 9, and 17 of the '011 Patent. *See* Ex. A.

Morong combined with Djenguerian renders obvious claims 1-3, 5-9, 11, 13, 16-18, 20-23, and 25-26 of the '486 Patent. *See* Ex. B.

c. Asserted Patents are Unenforceable Because of Power Integrations' Inequitable Conduct

While not specifically contemplated under the proposed schedule, CogniPower contends the Asserted Patents are unenforceable based on Power Integrations' inequitable conduct and thus includes the allegation in this disclosure. As pled in CogniPower's Answer (D.I. 19) and incorporated by reference, Power Integrations was aware of the application that led to Morong before the Asserted Patents issued. But Power Integrations did not disclose it to the USPTO. Instead, CogniPower pled that Power Integrations withheld this material information from the USPTO with the specific intent to deceive regarding that prior art with respect to the Asserted Patents. Thus, all the claims of the Asserted Patents are unenforceable.

II. DOCUMENT PRODUCTION ACCOMPANYING INVALIDITY CONTENTIONS

Along with these disclosures, CogniPower is producing relevant, non-privileged documents in compliance with paragraph 6 of the proposed scheduling order. D.I. 25-1. CogniPower reserves the right to supplement its production as necessary as the case progresses.

Dated: December 9, 2020

COLE SCHOTZ P.C.

/s/ Michael F. Bonkowski

Michael F. Bonkowski (No. 2219)

Andrew L. Cole (No. 5712)

500 Delaware Avenue, Suite 1410

Wilmington, DE 19801

T: 302.652.3131

F: 302.652.3117

mbonkowski@coleschotz.com

acole@coleschotz.com

Gary R. Sorden (admitted *pro hac vice*)

Niky R. Bagley (admitted *pro hac vice*)

Timothy J.H. Craddock (admitted *pro hac vice*)

James R. Perkins (admitted *pro hac vice*)

COLE SCHOTZ P.C.

901 Main Street, Suite 4120

Dallas, Texas 75202

T: 469.557.9390

F: 469.533.1587

gsorden@coleschotz.com

nbagley@coleschotz.com

tcraddock@coleschotz.com

jperkins@coleschotz.com

*Attorneys for Defendant,
CogniPower LLC*

EXHIBIT A

**Invalidity Claim Chart for U.S. Patent No. 9,374,011 (Liu)
SECONDARY CONTROLLER FOR USE IN SYNCHRONOUS FLYBACK CONVERTER**

Motivation to Combine: FIG. 4 of U.S. Pat. No. 9,071,152 (Morong) shows a flyback power converter that performs secondary-side rectification using a diode. Based on the well-known advantages provided by active secondary-side rectification (as taught, for example, in U.S. Pat. No. 7,385,832 (Allinder)), it would have been obvious to a person skilled in the art to modify FIG. 4 of Morong to perform secondary-side rectification using a synchronous rectification (SR) switch as taught in Allinder (and many other prior-art references). Note that, like Liu, FIG. 4 of Morong has a secondary-side drive circuit that generates a drive signal that turns on a primary-side switch. Allinder does not teach such a secondary-side drive circuit. Rather, Allinder teaches a flyback power converter having a primary-side drive circuit that generates a drive signal that controls a primary-side switch. Nevertheless, it would have been obvious to modify Morong's flyback power converter 10d of FIG. 4 with the addition of secondary-side rectification using an SR switch based, at least, on Allinder's teachings.

EXHIBIT A

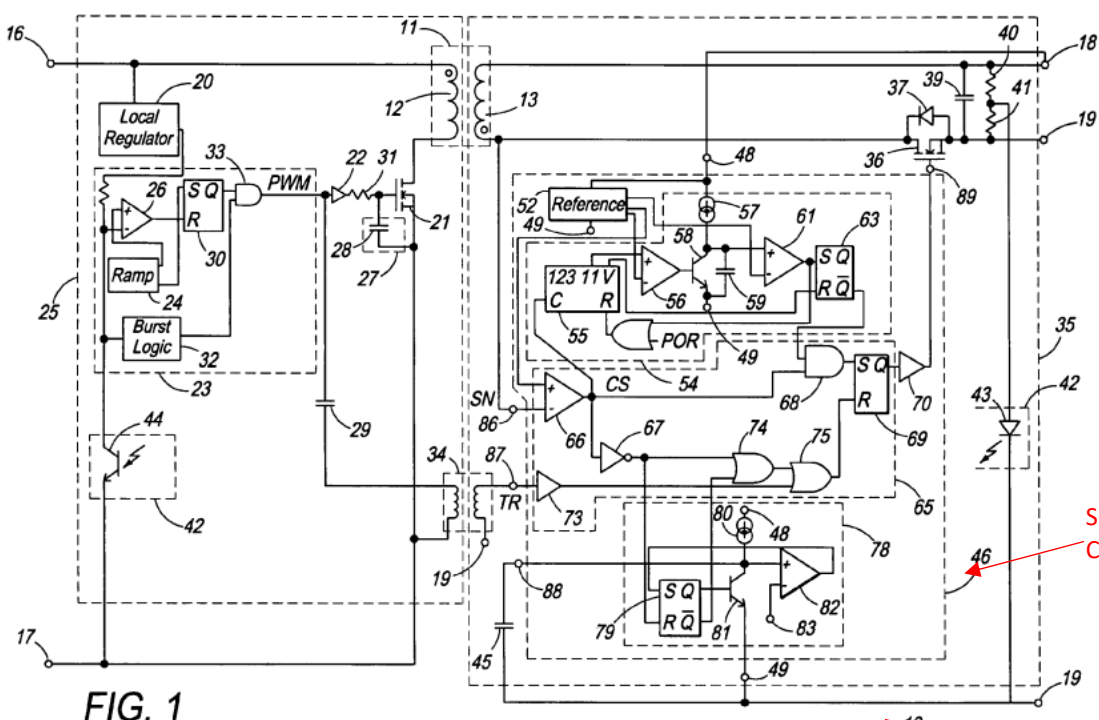
| U.S. Pat. No. 9,374,011 | U.S. Pat. No. 7,385,832 (Allinder) + U.S. Pat. No. 9,071,152 (Morong) |
|---|--|
| <p>1. A secondary controller for use in a synchronous flyback converter, the secondary controller comprising:</p> | <p>Fig. 1 of Allinder below discloses a secondary controller (secondary-side power supply controller 46) for use in a synchronous flyback converter (power supply system 10).</p>  <p style="text-align: center;">FIG. 1</p> <p style="text-align: center;">Synchronous Flyback Converter → 10</p> <p style="text-align: right;">Secondary Controller → 46</p> |
| <p>a comparator coupled to generate a compare signal in response to a</p> | <p>Fig. 1 in Allinder below discloses a comparator (comparator 66) coupled to generate a compare signal (CS signal) in response to a comparison of a threshold (voltage from reference 52) to an</p> |

EXHIBIT A

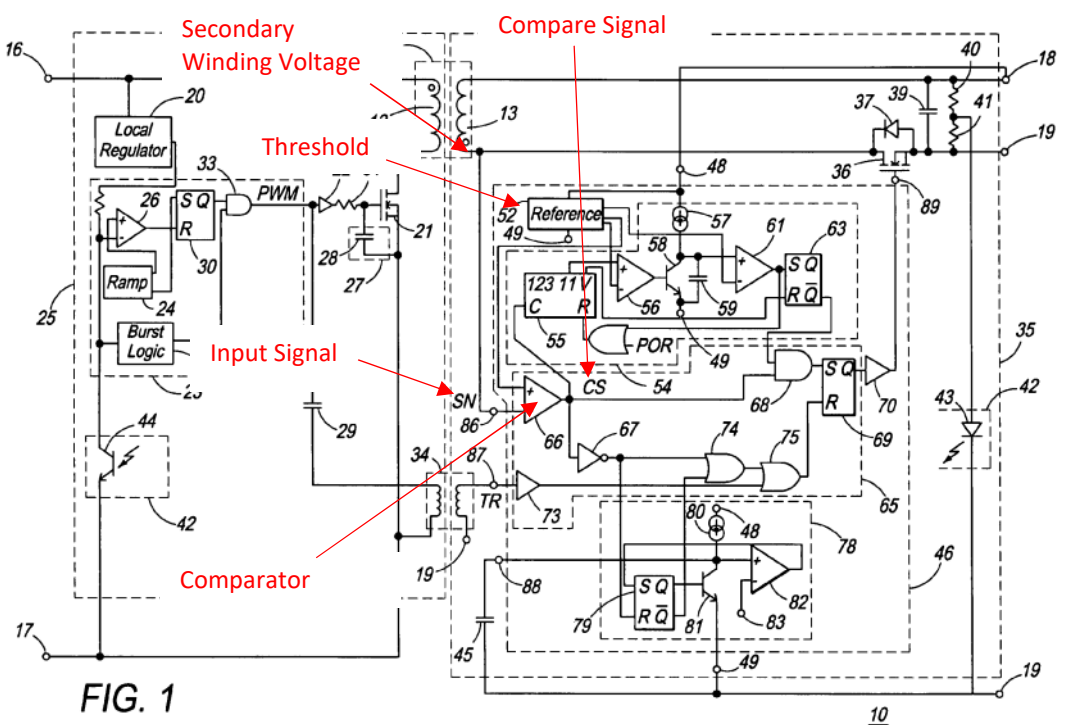
| | |
|--|---|
| U.S. Pat. No. 9,374,011 | U.S. Pat. No. 7,385,832 (Allinder) + U.S. Pat. No. 9,071,152 (Morong) |
| <p>comparison of a threshold to an input signal representative of a secondary winding voltage of the synchronous flyback converter;</p> | <p>input signal (SN signal) representative of a secondary winding voltage (voltage at the bottom of secondary winding 13) of the synchronous flyback converter (power supply system 10).</p>  <p>FIG. 1</p> <p>Synchronous Flyback Converter</p> |
| <p>a drive circuit coupled to generate a drive signal to control a first switch to be coupled to a primary side of the synchronous flyback converter, wherein the drive signal</p> | <p>Fig. 4 in Morong below discloses a drive circuit (at least elements 412d, 414d, 415d, 507d, 508d, 509d) coupled to generate a drive signal (the output of NAND gate 509d) to control (turn on) a first switch (switch 200d) to be coupled to a primary side of the synchronous flyback converter (power converter 10d), wherein the drive signal (output of NAND gate 509d) is coupled to be generated by the drive circuit (at least elements 412d, 414d, 415d, 507d, 508d, 509d) in response</p> |

EXHIBIT A

U.S. Pat. No. 9,374,011

is coupled to be generated by the drive circuit in response to a feedback signal representative of an output of the synchronous flyback converter; and

U.S. Pat. No. 7,385,832 (Allinder) + U.S. Pat. No. 9,071,152 (Morong)

to a feedback signal (voltage at node between resistors 408d and 409d) representative of an output (voltage at terminal 13d) of the synchronous flyback converter (power converter 10d).

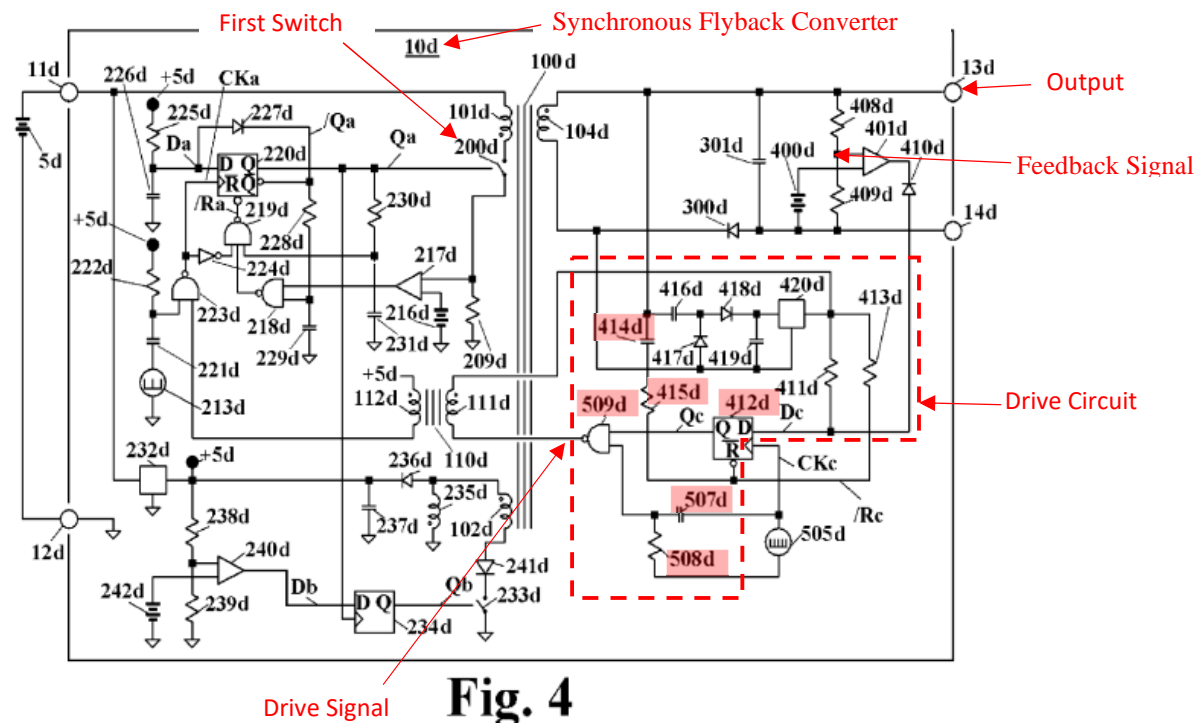


EXHIBIT A

| U.S. Pat. No. 9,374,011 | U.S. Pat. No. 7,385,832 (Allinder) + U.S. Pat. No. 9,071,152 (Morong) |
|---|--|
| <p>logic circuitry coupled to the drive circuit and coupled to the comparator, wherein the logic circuitry is coupled to generate a control signal to control a second switch in response to the drive signal and in response to the compare signal, and wherein the second switch is to be coupled to a secondary side of the synchronous flyback converter.</p> | <p>As described in the next paragraph, the secondary controller (secondary-side power supply controller 46) shown in Fig. 1 of Allinder has examples of the logic circuitry and comparator, but Allinder's drive circuit (PWM controller 23) is on the primary side of Allinder's synchronous flyback converter (power supply system 10), not on the secondary side. Nevertheless, Allinder's primary-side drive signal (PWM control signal) is applied to Allinder's secondary-side logic circuit via the TR signal at input 87.</p> <p>Fig. 1 in Allinder below discloses a logic circuitry (at least elements 68, 69, 74, and 75) coupled to the drive circuit (PWM controller 23) and coupled to the comparator (at least comparator 66), wherein the logic circuitry is coupled to generate a control signal (output 89) to control a second switch (transistor 36) in response to the drive signal (PWM control signal) and in response to the compare signal (CS signal), and wherein the second switch is to be coupled to a secondary side of the synchronous flyback converter (power supply system 10).</p> |

EXHIBIT A

| U.S. Pat. No. 9,374,011 | U.S. Pat. No. 7,385,832 (Allinder) + U.S. Pat. No. 9,071,152 (Morong) |
|---|---|
| | <p>FIG. 1 Drive Circuit</p> <p>Second Switch</p> <p>Control Signal</p> <p>Logic Circuitry</p> <p>Comparator</p> <p>Drive Signal</p> <p>Compare Signal</p> <p>Synchronous Flyback Converter</p> |
| <p>8. The secondary controller of claim 1 further comprising an oscillator coupled to generate a clock signal coupled to be received by the drive circuit, wherein the drive circuit is coupled to generate</p> | <p>Fig. 4 in Morong below discloses an oscillator (oscillator 505d) coupled to generate a clock signal (the signal at node CKc) coupled to be received by the drive circuit (at least elements 412d, 414d, 415d, 507d, 508d, 509d), wherein the drive circuit is coupled to generate the drive signal (the output of NAND gate 509d) in response to the clock signal.</p> |

EXHIBIT A

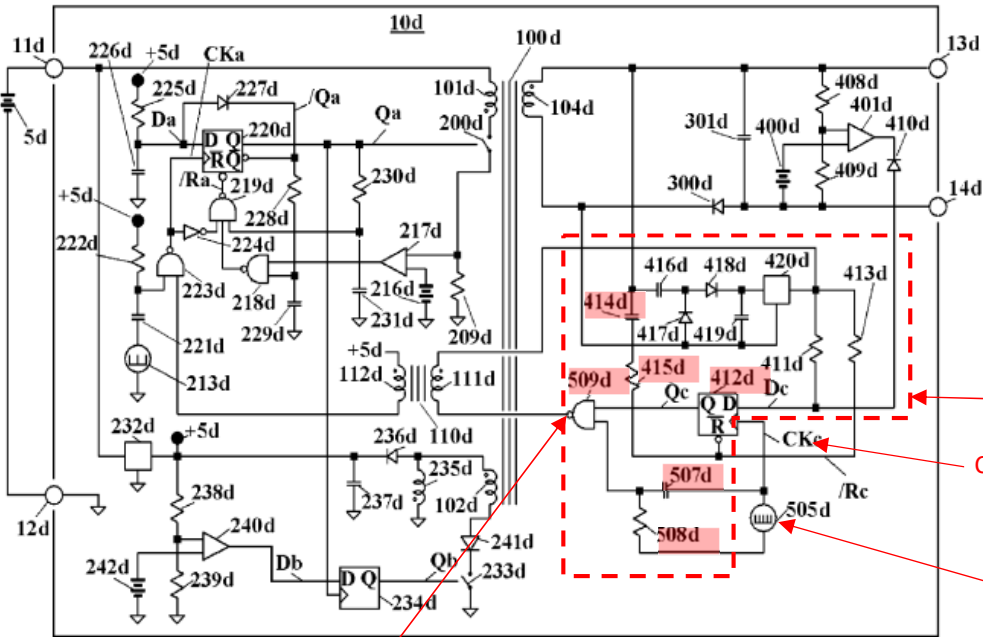
| U.S. Pat. No. 9,374,011 | U.S. Pat. No. 7,385,832 (Allinder) + U.S. Pat. No. 9,071,152 (Morong) |
|---|---|
| <p>the drive signal in response to the clock signal.</p> |  <p>The diagram illustrates a power converter circuit. It includes an oscillator section (505d, 507d, 508d, 509d) generating a clock signal (CKe). This signal is processed through a drive circuit (411d, 412d, 413d, 414d, 415d, 416d, 417d, 418d, 419d, 420d) to produce a drive signal. The drive signal is then used to control a power stage (100d) consisting of a primary winding (101d, 200d) and a secondary winding (104d). The secondary winding is connected to a load (13d, 14d). The circuit also includes various other components like transistors (Qa, Qb, Qc), diodes (Da, Db, Dc), resistors (Rc, 219d, 220d, 221d, 222d, 223d, 224d, 225d, 226d, 227d, 228d, 229d, 230d, 231d, 232d, 233d, 234d, 235d, 236d, 237d, 238d, 239d, 240d, 241d, 242d), capacitors (112d, 110d, 102d, 104d, 300d, 301d, 400d, 408d, 409d, 410d), and a transformer (111d, 112d, 101d, 200d, 104d, 100d). The circuit is powered by a +5d supply (11d, 12d, 13d, 14d).</p> <p>Fig. 4</p> |
| <p>9. A power converter, comprising:</p> | <p>Both Allinder (power supply system 10 of Fig. 1) and Morong (power converter 10d of Fig. 4) disclose a power converter.</p> |
| <p>an energy transfer element having a primary winding and a secondary winding;</p> | <p>Both Allinder and Morong disclose an energy transfer element having a primary winding and a secondary winding.</p> |

EXHIBIT A

U.S. Pat. No. 9,374,011

U.S. Pat. No. 7,385,832 (Allinder) + U.S. Pat. No. 9,071,152 (Morong)

Fig. 1 in Allinder below discloses an energy transfer element (transformer 11) having a primary winding (primary side inductor 12) and a secondary winding (secondary side inductor 13).

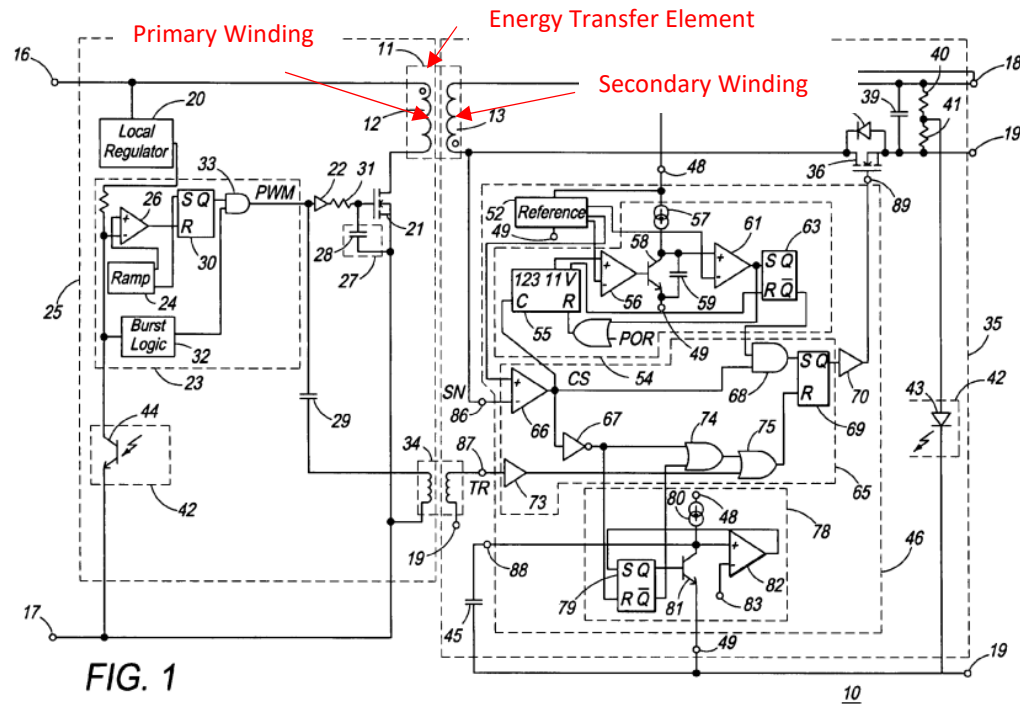


FIG. 1

EXHIBIT A

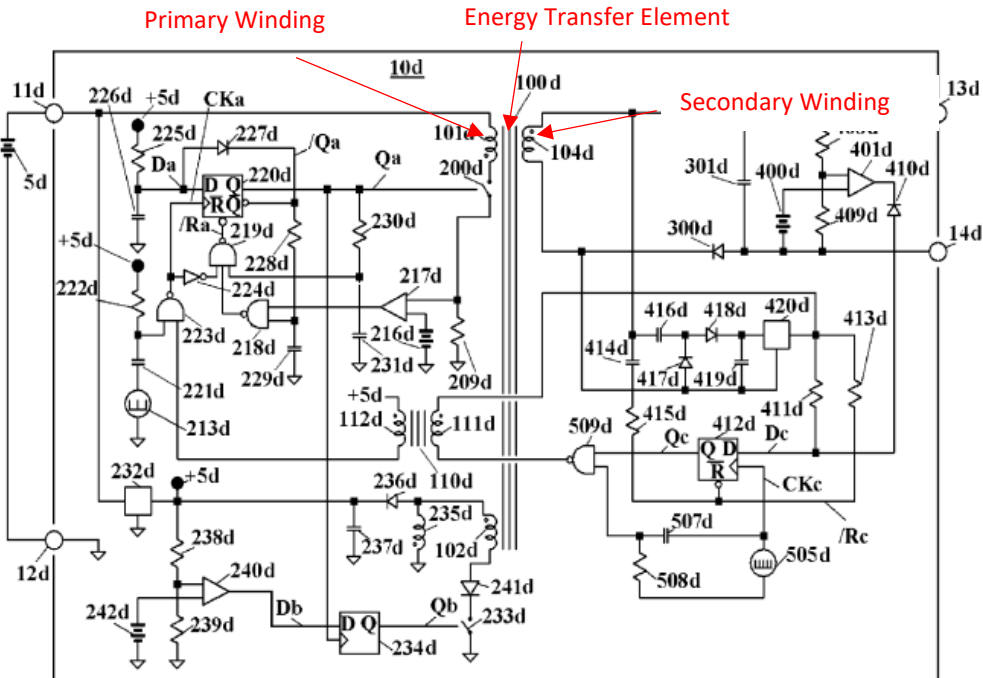
| U.S. Pat. No. 9,374,011 | U.S. Pat. No. 7,385,832 (Allinder) + U.S. Pat. No. 9,071,152 (Morong) |
|---|--|
| | <p>Fig. 4 in Morong below discloses an energy transfer element (transformer 100d) having a primary winding (primary winding 101d) and a secondary winding (secondary winding 104d).</p>  <p style="text-align: center;">Fig. 4</p> |
| a first switch coupled to the primary winding and coupled to an input of the power converter; and | Both Allinder and Morong disclose a first switch coupled to the primary winding and coupled to an input of the power converter. |

EXHIBIT A

U.S. Pat. No. 9,374,011

U.S. Pat. No. 7,385,832 (Allinder) + U.S. Pat. No. 9,071,152 (Morong)

Fig. 1 in Allinder below discloses a first switch (transistor 21) coupled to the primary winding (primary side inductor 12) and coupled to an input (terminals 16 and 17) of the power converter (power supply system 10).

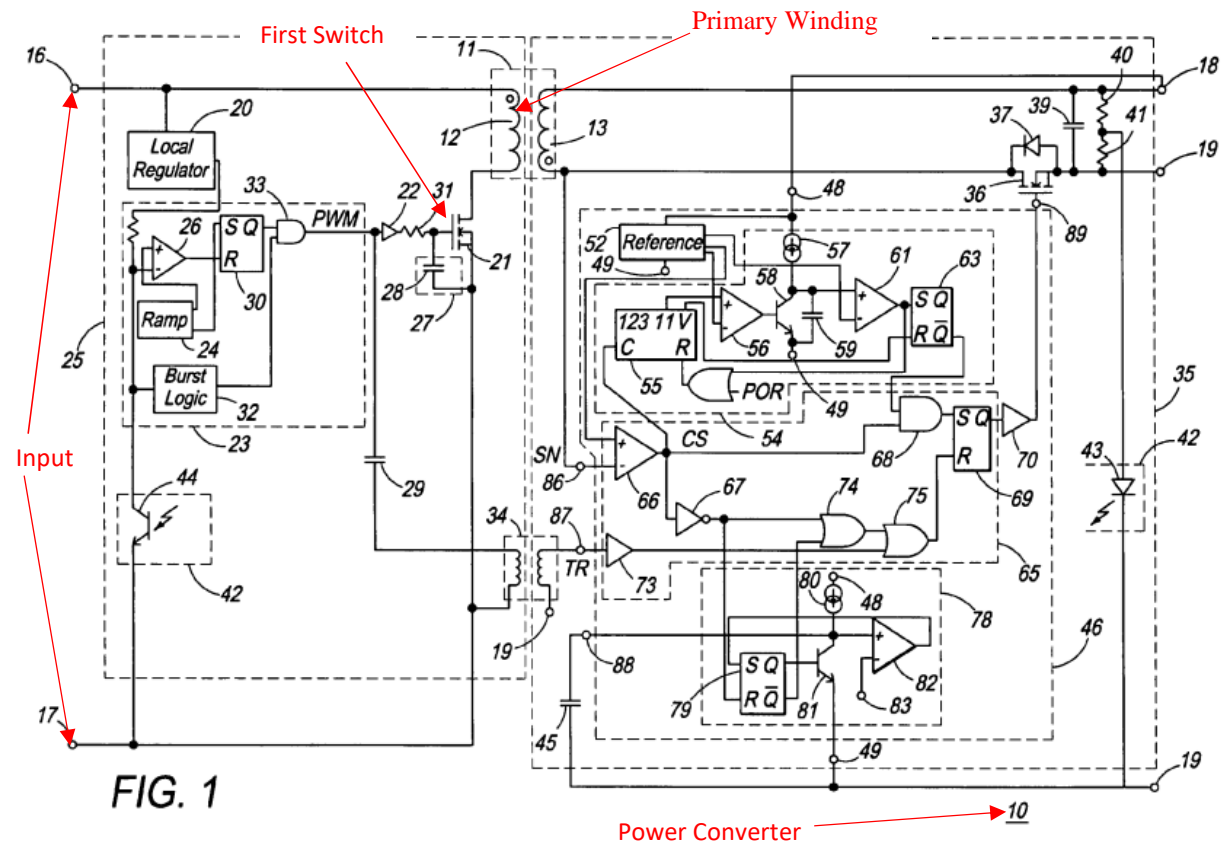


EXHIBIT A

| | |
|--------------------------------|--|
| <p>U.S. Pat. No. 9,374,011</p> | <p>U.S. Pat. No. 7,385,832 (Allinder) + U.S. Pat. No. 9,071,152 (Morong)</p> |
| | <p>Fig. 4 in Morong below discloses a first switch (switch 200d) coupled to the primary winding (primary winding 101d) and coupled to an input (terminals 11d and 12d) of the power converter (power converter 10d).</p> |

EXHIBIT A

| | |
|---|--|
| <p>U.S. Pat. No. 9,374,011</p> | <p>U.S. Pat. No. 7,385,832 (Allinder) + U.S. Pat. No. 9,071,152 (Morong)</p> |
| <p>a secondary controller coupled to control switching of the first switch to control a transfer of energy through the energy transfer element from the input of the power converter to an output of the power converter, the secondary controller including:</p> | <p>Fig. 4 in Morong below discloses a secondary controller (elements 411d-509d) coupled to control switching of the first switch (switch 200d) to control a transfer of energy through the energy transfer element (transformer 100d) from the input of the power converter (terminals 11d and 12d) to an output of the power converter (terminals 13d and 14d).</p> |

EXHIBIT A

U.S. Pat. No. 9,374,011

input signal representative of a secondary winding voltage of the secondary winding;

U.S. Pat. No. 7,385,832 (Allinder) + U.S. Pat. No. 9,071,152 (Morong)

52) to an input signal (SN signal) representative of a secondary winding voltage (voltage at bottom of secondary winding 13) of the secondary winding (secondary winding 13).

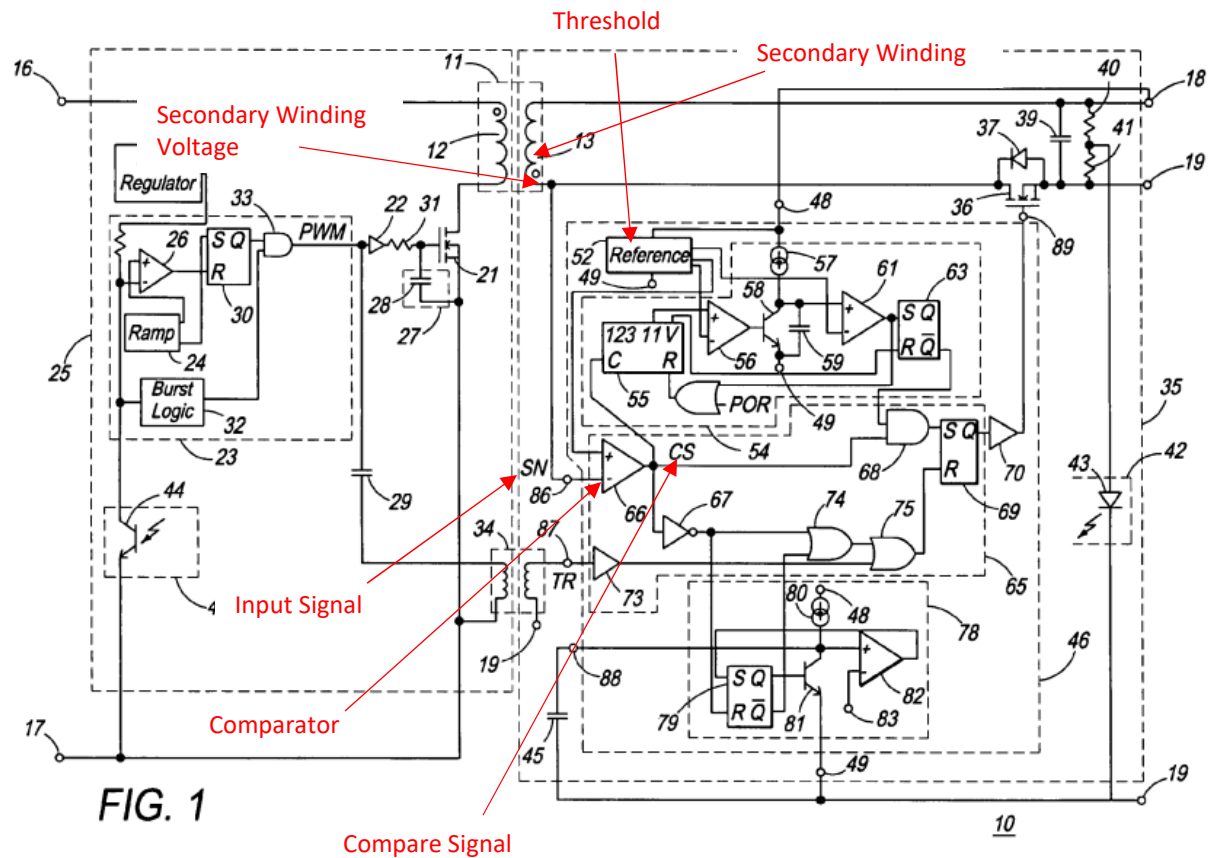


EXHIBIT A

| | |
|---|--|
| <p>U.S. Pat. No. 9,374,011</p> | <p>U.S. Pat. No. 7,385,832 (Allinder) + U.S. Pat. No. 9,071,152 (Morong)</p> |
| <p>a drive circuit coupled to generate a drive signal to control the first switch, wherein the drive signal is coupled to be generated by the drive circuit in response to a feedback signal representative of the output of the power converter; and</p> | <p>Fig. 4 of Morong below discloses a drive circuit (at least elements 412d, 414d, 415d, 507d, 508d, 509d) coupled to generate a drive signal (output of NAND gate 509d) to control (turn on) the first switch (switch 200d), wherein the drive signal is coupled to be generated by the drive circuit in response to a feedback signal (voltage at node between resistors 408d and 409d) representative of the output (voltage at terminal 13) of the power converter (power converter 10d).</p> <p>Fig. 4</p> |

EXHIBIT A

| U.S. Pat. No. 9,374,011 | U.S. Pat. No. 7,385,832 (Allinder) + U.S. Pat. No. 9,071,152 (Morong) |
|---|---|
| <p>logic circuitry coupled to the drive circuit and coupled to the comparator, wherein the logic circuitry is coupled to generate a control signal to control a second switch in response to the drive signal and in response to the compare signal, and wherein the second switch is coupled to a secondary side of the power converter.</p> | <p>As described in the next paragraph, the secondary controller (secondary-side power supply controller 46) shown in Fig. 1 of Allinder has examples of the logic circuitry and comparator, but Allinder's drive circuit (PWM controller 23) is on the primary side of Allinder's synchronous flyback converter (power supply system 10), not on the secondary side. Nevertheless, Allinder's primary-side drive signal (PWM control signal) is applied to Allinder's secondary-side logic circuit via the TR signal at input 87.</p> <p>Fig. 1 of Allinder below discloses a logic circuitry (at least elements 68, 69, 74, and 75) coupled to the drive circuit (PWM controller 23) and coupled to the comparator (comparator 66), wherein the logic circuitry is coupled to generate a control signal (output 89) to control a second switch (transistor 36) in response to the drive signal (PWM control signal) and in response to the compare signal (CS signal), and wherein the second switch (transistor 36) is coupled to a secondary side of the power converter (power supply system 10).</p> |

EXHIBIT A

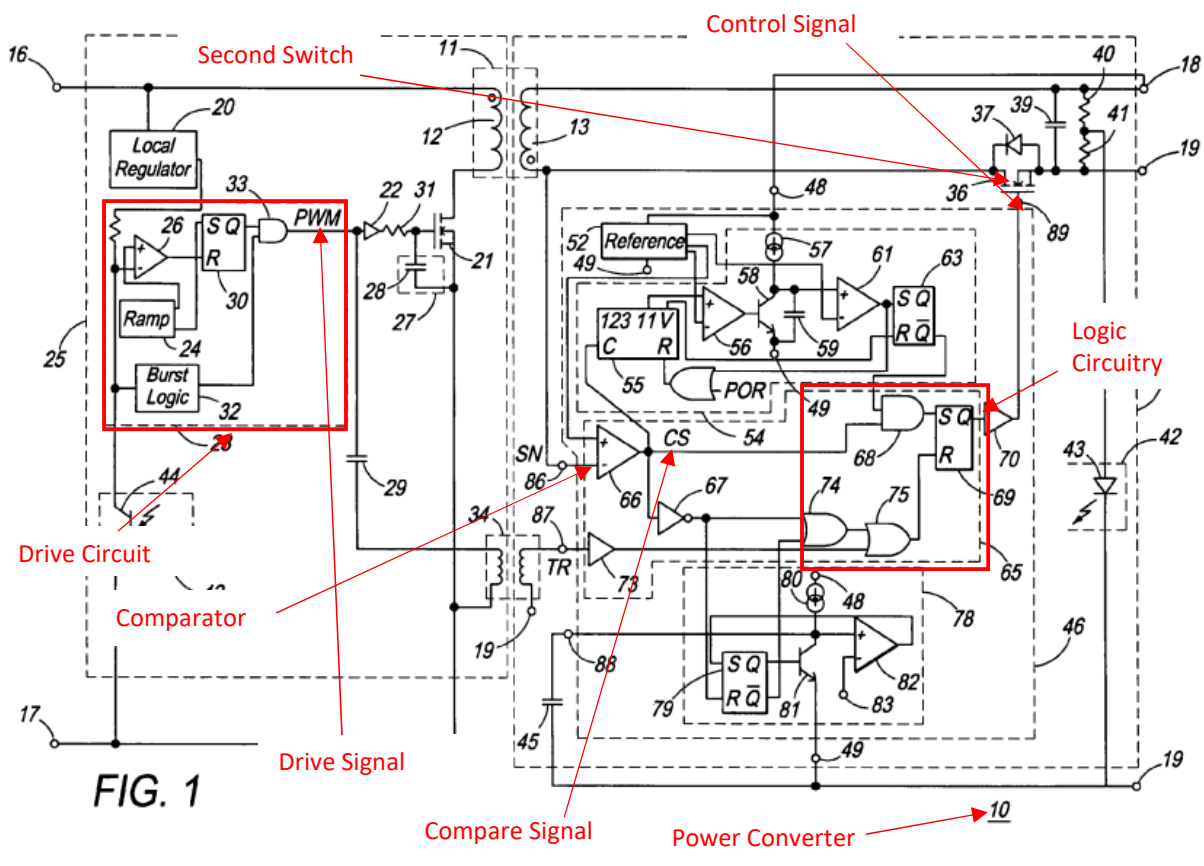
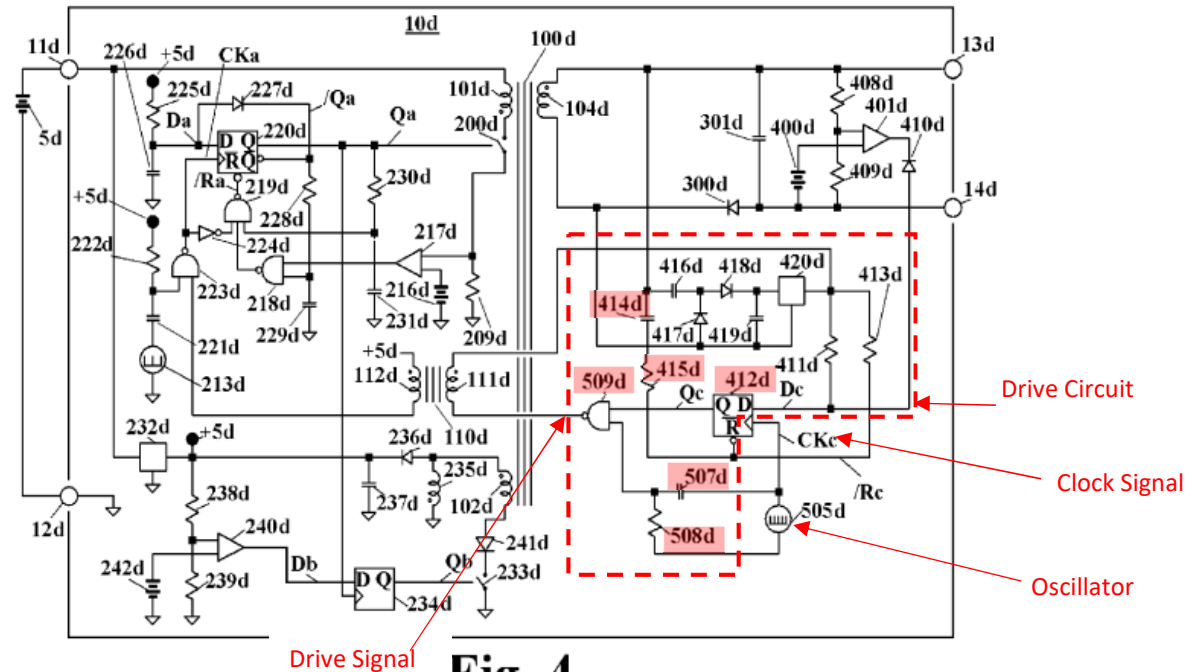
| U.S. Pat. No. 9,374,011 | U.S. Pat. No. 7,385,832 (Allinder) + U.S. Pat. No. 9,071,152 (Morong) |
|---|--|
| |  <p>The diagram shows a power converter system with various components and signals. Key elements include:</p> <ul style="list-style-type: none"> FIG. 1: A schematic diagram of a power converter system. Annotations: Red arrows point to specific components and signals: <ul style="list-style-type: none"> Second Switch: Points to component 11. Control Signal: Points to component 40. Logic Circuitry: Points to a block containing components 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100. Drive Circuit: Points to a block containing components 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100. Comparator: Points to component 26. Drive Signal: Points to component 28. Compare Signal: Points to component 86. Power Converter: Points to component 10. |
| <p>17. The power converter of claim 9 wherein the secondary controller further comprises an oscillator coupled to generate a clock signal</p> | <p>Figure 4 in Morong below discloses an oscillator (oscillator 505d) coupled to generate a clock signal (signal at node CKc) coupled to be received by the drive circuit, wherein the drive circuit (at least elements 412d, 414d, 415d, 507d, 508d, 509d) is coupled to generate the drive signal (output of NAND gate 509d) in response to the clock signal.</p> |

EXHIBIT A

U.S. Pat. No. 9,374,011

coupled to be received by the drive circuit, wherein the drive circuit is coupled to generate the drive signal in response to the clock signal.

U.S. Pat. No. 7,385,832 (Allinder) + U.S. Pat. No. 9,071,152 (Morong)



EXHBIT B

**Claim Chart for U.S. Patent No. 9,166,486
POWER CONVERTER USING MULTIPLE CONTROLLERS**

Motivation to Combine: FIG. 4 of U.S. Pat. No. 9,071,152 (Morong) shows a flyback power converter that varies the frequency of power cycling of the flyback converter with the load, where each power cycle involves turning on and then turning off the primary-side power switch when a threshold current limit is reached. It may be advantageous to avoid certain frequencies of operation, such as those in the audible range. It would have been obvious to a POSITA that, for a given load, (i) the operating frequency range of the power converter can be controlled by changing the amount of energy transferred with each power cycle, (ii) the amount of energy transferred per power cycle can be controlled by changing the ON time of the power switch (i.e., the duration that the power switch remains on during each power cycle), and (iii) the ON time can be controlled by adjusting the threshold current limit used to determine when to turn off the power switch. Therefore, it would be obvious to a POSITA to modify Fig. 4 of Morong to adjust the threshold current limit in response to an amount of time the power switch is in the ON state as taught in U.S. Pat. No. 7,746,050 (Djenguerian) in order to control the frequency of operation of the flyback power converter to cause the power converter to operate in a desired frequency range.

EXHIBIT B

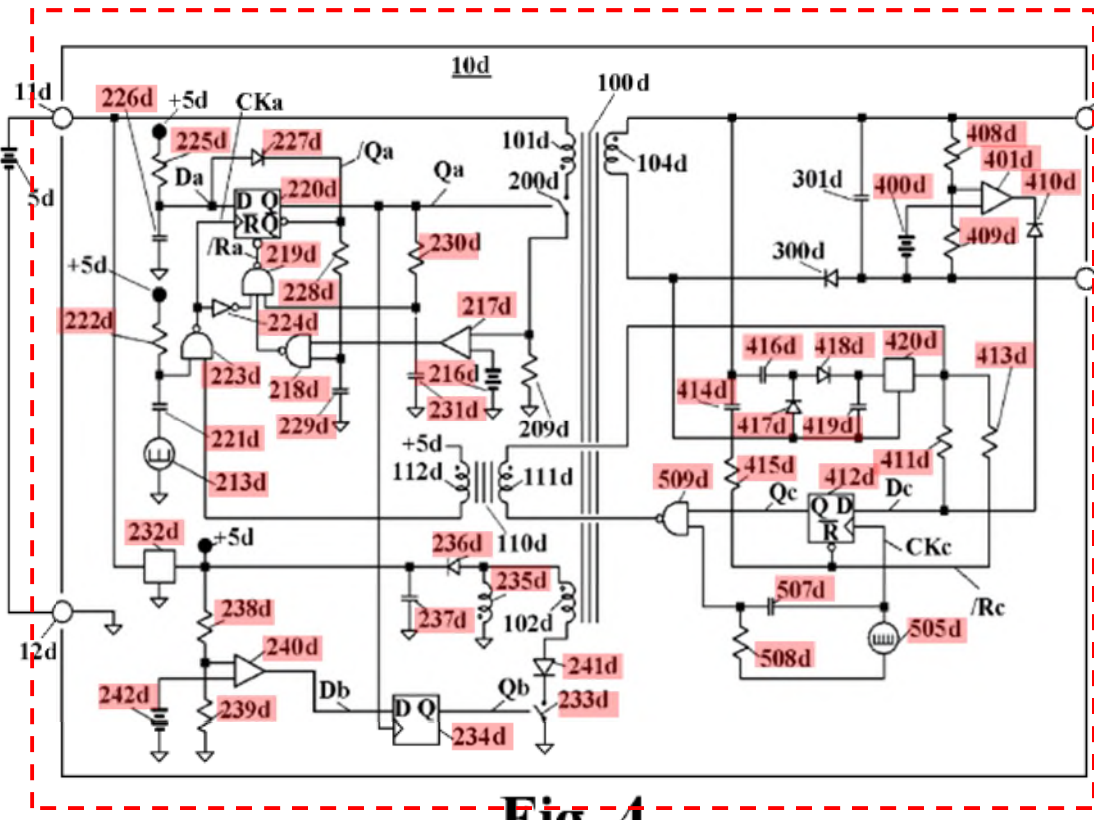
| | |
|--|---|
| <p>U.S. Pat. No. 9,166,486</p> | <p>U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian)</p> |
| <p>1. A power converter controller comprising:</p> | <p>Fig. 4 in Morong shows a power converter controller (elements 213d-242d and 400d-509d).</p>  <p style="text-align: center;">Fig. 4</p> |
| <p>a primary controller to be coupled to a power</p> | <p>Fig. 4 in Morong shows a primary controller (elements 213d-242d) to be coupled to a power switch (switch 200d) of a power converter (power controller 10d), wherein the primary controller is coupled to</p> |

EXHIBIT B

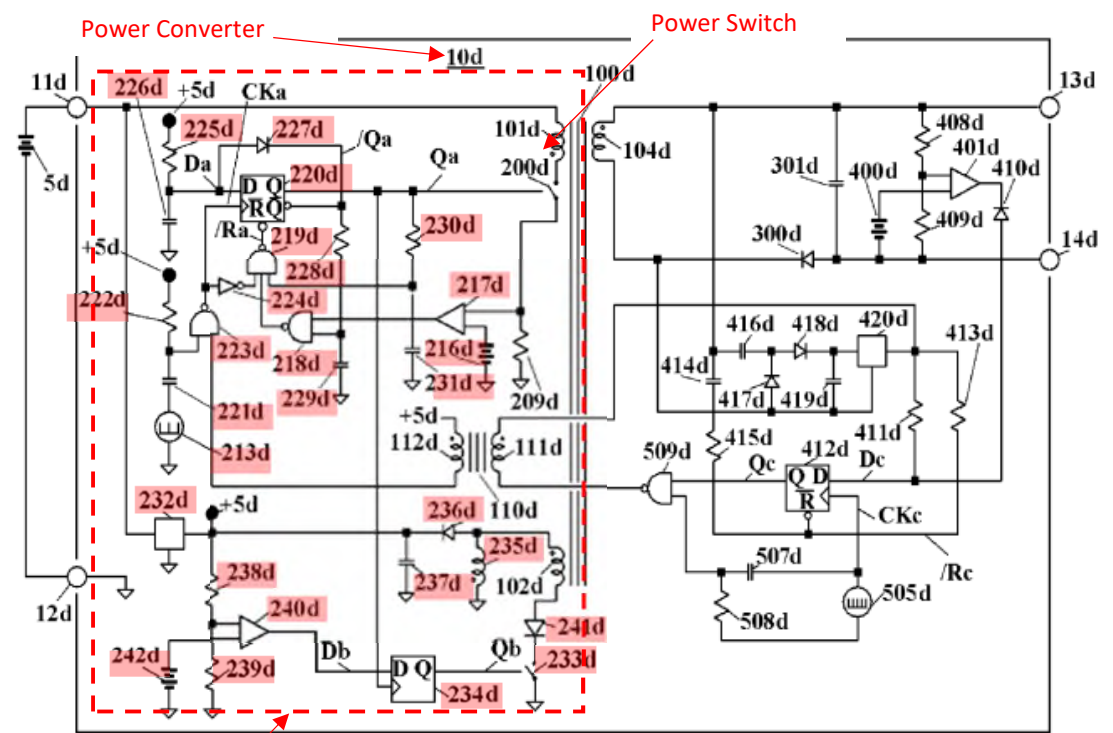
| | |
|---|---|
| <p>U.S. Pat. No. 9,166,486</p> | <p>U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian)</p> |
| <p>switch of a power converter, wherein the primary controller is coupled to receive one or more request signals and transition the power switch from an OFF state to an ON state in response to each of the one or more received request signals, and wherein the primary controller is coupled to detect a turn-off condition when the power switch is in the ON state and transition the power switch from the ON state to the OFF state in response to detection of the turn-off condition; and</p> | <p>receive one or more request signals (demand pulses) and transition the power switch from an OFF state to an ON state in response to each of the one or more received request signals, and wherein the primary controller is coupled to detect a turn-off condition when the power switch is in the ON state and transition the power switch from the ON state to the OFF state in response to detection of the turn-off condition.</p>  <p>The diagram illustrates a control system for a power converter. It is divided into three main functional blocks: the Primary Controller, the Power Converter, and the Power Switch.</p> <ul style="list-style-type: none"> Primary Controller (Left): This block contains a microcontroller (210d) and various logic components including comparators (217d, 218d), logic gates (219d, 220d, 221d, 222d, 223d, 224d, 225d, 226d, 227d, 228d, 229d, 230d, 231d, 232d, 233d, 234d, 235d, 236d, 237d, 238d, 239d, 240d, 241d, 242d), and flip-flops (211d, 212d, 213d, 214d, 215d, 216d, 217d, 218d, 219d, 220d, 221d, 222d, 223d, 224d, 225d, 226d, 227d, 228d, 229d, 230d, 231d, 232d, 233d, 234d, 235d, 236d, 237d, 238d, 239d, 240d, 241d, 242d). It also includes a reference voltage source (210d) and a feedback network (211d, 212d, 213d, 214d, 215d, 216d, 217d, 218d, 219d, 220d, 221d, 222d, 223d, 224d, 225d, 226d, 227d, 228d, 229d, 230d, 231d, 232d, 233d, 234d, 235d, 236d, 237d, 238d, 239d, 240d, 241d, 242d). Power Converter (Middle): This block contains a transformer (100d) with primary and secondary windings (101d, 102d, 103d, 104d, 105d, 106d, 107d, 108d, 109d, 110d, 111d, 112d, 113d, 114d, 115d, 116d, 117d, 118d, 119d, 120d, 121d, 122d, 123d, 124d, 125d, 126d, 127d, 128d, 129d, 130d, 131d, 132d, 133d, 134d, 135d, 136d, 137d, 138d, 139d, 140d, 141d, 142d, 143d, 144d, 145d, 146d, 147d, 148d, 149d, 150d, 151d, 152d, 153d, 154d, 155d, 156d, 157d, 158d, 159d, 160d, 161d, 162d, 163d, 164d, 165d, 166d, 167d, 168d, 169d, 170d, 171d, 172d, 173d, 174d, 175d, 176d, 177d, 178d, 179d, 180d, 181d, 182d, 183d, 184d, 185d, 186d, 187d, 188d, 189d, 190d, 191d, 192d, 193d, 194d, 195d, 196d, 197d, 198d, 199d, 200d, 201d, 202d, 203d, 204d, 205d, 206d, 207d, 208d, 209d, 210d, 211d, 212d, 213d, 214d, 215d, 216d, 217d, 218d, 219d, 220d, 221d, 222d, 223d, 224d, 225d, 226d, 227d, 228d, 229d, 230d, 231d, 232d, 233d, 234d, 235d, 236d, 237d, 238d, 239d, 240d, 241d, 242d). It also includes a feedback network (211d, 212d, 213d, 214d, 215d, 216d, 217d, 218d, 219d, 220d, 221d, 222d, 223d, 224d, 225d, 226d, 227d, 228d, 229d, 230d, 231d, 232d, 233d, 234d, 235d, 236d, 237d, 238d, 239d, 240d, 241d, 242d). Power Switch (Right): This block contains a MOSFET (300d) and a diode (301d). It also includes a feedback network (211d, 212d, 213d, 214d, 215d, 216d, 217d, 218d, 219d, 220d, 221d, 222d, 223d, 224d, 225d, 226d, 227d, 228d, 229d, 230d, 231d, 232d, 233d, 234d, 235d, 236d, 237d, 238d, 239d, 240d, 241d, 242d). <p>The diagram shows the interconnections between these blocks, including the flow of control signals and power. The primary controller (210d) is connected to the power converter (100d) and the power switch (300d). The power converter (100d) is connected to the power switch (300d). The power switch (300d) is connected to the load (13d, 14d). The feedback network (211d, 212d, 213d, 214d, 215d, 216d, 217d, 218d, 219d, 220d, 221d, 222d, 223d, 224d, 225d, 226d, 227d, 228d, 229d, 230d, 231d, 232d, 233d, 234d, 235d, 236d, 237d, 238d, 239d, 240d, 241d, 242d) provides feedback signals to the primary controller (210d).</p> <p>Fig. 4</p> |

EXHIBIT B

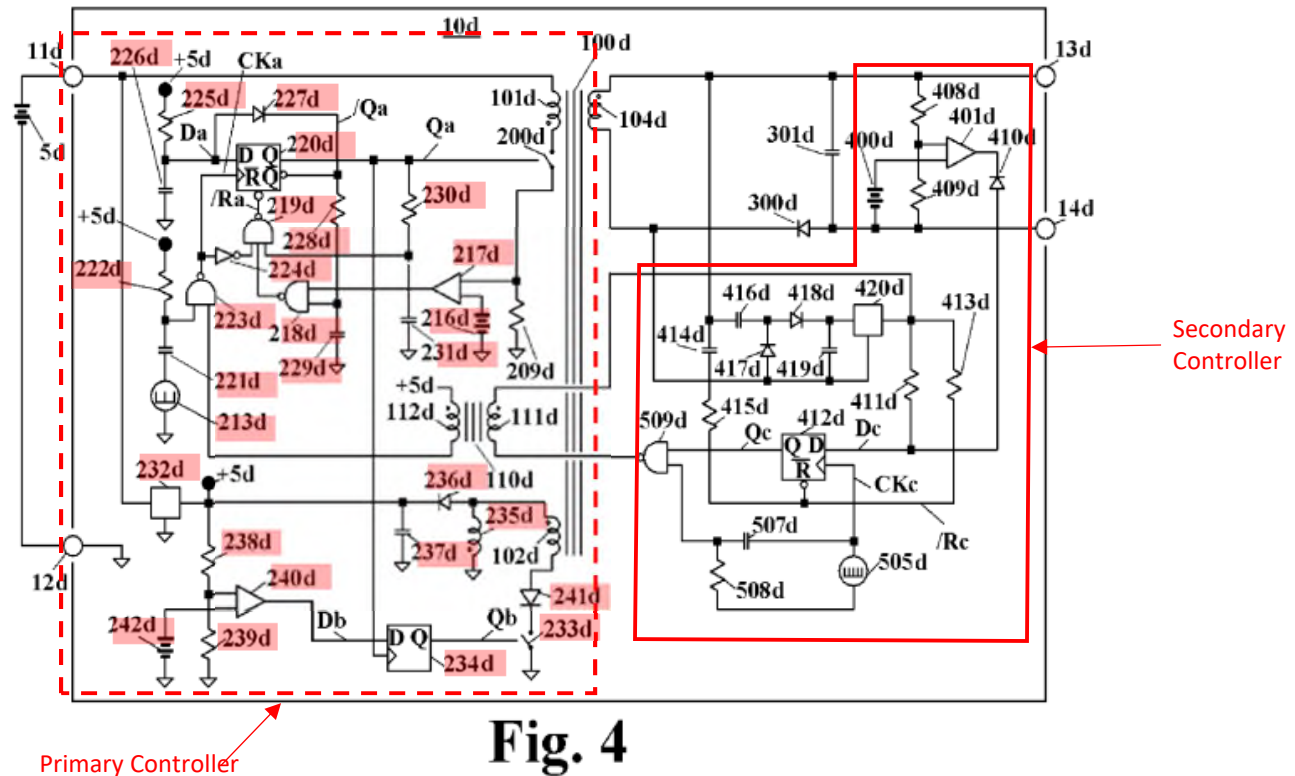
| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|--|---|
| | <p>As shown in FIG. 4, the primary controller (i.e., elements 213d-242d) is coupled to receive one or more demand pulses and transition the switch 200d from an OFF state to an ON state in response to each of the one or more demand pulses.</p> <p>“The ON pulses of switch 200d responsive to oscillator 213d are sufficiently frequent to start the converter of this embodiment, but insufficiently frequent to drive it to full output. To initiate more frequent pulses, an oscillator 505d drives a capacitor 507d and a resistor 508d to supply differentiated pulses of about 100 nS width to a NAND gate 509d, which in turn drives a primary winding 111d of demand pulse transformer 110d, thus producing demand pulses across a secondary winding 112d thereof. These winding 112d pulses are conveyed through a NAND gate 223d to clock flip-flop 220d at up to the frequency of oscillator 505d.” 7:42-52.</p> <p>“If all of the pulses of oscillator 505d were allowed to clock flip-flop 220d, under some conditions, the converter of this embodiment would produce excess output. To regulate this output, a flip-flop 412d is used to gate the pulses passed by NAND gate 509d. At a node CKc, oscillator 505d clocks a flip-flop 412d, which generates a logic high at a node Qc only when a logic high is present at a node Dc at the rising edge of its clock. Thus, pulses driving transformer 110d are permitted responsive to a logic high only at node Dc.” 7:53-61.</p> <p>As shown in FIG. 4, the primary controller (i.e., elements 213d-242d) are coupled to detect a turn-off condition when the switch 200d is in the ON state and transition the switch 200d from the ON state to the OFF state in response to detection of the turn-off condition.</p> <p>“When current in resistor 209d exceeds a value set by reference 216d, comparator 217d issues a reset signal which propagates through NAND gates 218d and 219d to a node /Ra where the reset signal resets flip-flop 220d, turning OFF switch 200d.” 7:1-5.</p> |
| a secondary controller galvanically isolated | Fig. 4 of Morong shows a secondary controller (elements 400d-509d) galvanically isolated from the primary controller elements (213d-242d), wherein the secondary controller is coupled to transmit the one |

EXHIBIT B**U.S. Pat. No. 9,166,486**

from the primary controller, wherein the secondary controller is coupled to transmit the one or more request signals to the primary controller, and wherein the secondary controller is coupled to control an amount of time between the transmission of each of the request signals,

U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian)

or more request signals to the primary controller (elements 213d-242d), and wherein the secondary controller is coupled to control an amount of time between the transmission of each of the request signals (7:53-61).



“FIG. 4 shows a schematic diagram of a power converter 10d, comprising a separate transformer 110d to transmit demand pulses across a galvanic isolation barrier.” 6:37-39.

EXHIBIT B

| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|--|---|
| | <p>“If all of the pulses of oscillator 505d were allowed to clock flip-flop 220d, under some conditions, the converter of this embodiment would produce excess output. To regulate this output, a flip-flop 412d is used to gate the pulses passed by NAND gate 509d. At a node CKc, oscillator 505d clocks a flip-flop 412d, which generates a logic high at a node Qc only when a logic high is present at a node Dc at the rising edge of its clock. Thus, pulses driving transformer 110d are permitted responsive to a logic high only at node Dc.” 7:53-61.</p> |
| <p>wherein the turn-off condition is a threshold current limit and the primary controller is coupled to adjust the threshold current limit in response to an amount of time the power switch is in the ON state.</p> | <p>As shown in FIG. 4 of Morong, the turn-off condition is a threshold current limit (value set by reference 216d).</p> <p>“When current in resistor 209d exceeds a value set by reference 216d, comparator 217d issues a reset signal which propagates through NAND gates 218d and 219d to a node /Ra where the reset signal resets flip-flop 220d, turning OFF switch 200d.”</p> <p>To the extent that Power Integrations argues that Morong does not show that it adjusts the value set by reference 216d, then Djenguerian alone or in combination with Morong meets this limitation.</p> <p>Fig. 1 in Djenguerian shows a power converter (flyback power converter 100) wherein the turn-off condition is a threshold current limit and the primary controller (control circuit 115) is coupled to adjust the threshold current limit in response to an amount of time the power switch (power switch 105) is in the ON state.</p> |

EXHIBIT B

FIG. 1

As taught in Djenguerian, the turn-off condition is the power switch protective current limit threshold and the control circuit 115 is coupled to adjust the power switch protective current limit threshold in response to an amount of time the power switch 105 is in the ON state.

EXHIBIT B

| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|---|--|
| | <p>“In one example controller 115 is coupled to adjust a duty cycle of the power switch 105 to be proportional to a value of the input voltage signal multiplied by the time it takes for the current flowing in the power switch to change between two current values when the power switch is in the on state.” 4:48-53.</p> <p>“It is noted that although the above description employs the power switch switching period as the control parameter for adjustment based on the measured value of the (KVIN×t) product, more generally the ratio of the power switch on time to the power switch off time during any power switch switching cycle period, known as the power switch duty cycle, is a broader description of the same control functionality. In general, the power switch duty cycle can be adjusted by adjusting the power switch switching cycle period but also by other techniques including adjusting the power switch protective current limit threshold, directly controlling the period of time for which the power switch is on during each switching cycle period, on/off control, pulse width modulation or other suitable power converter switching techniques.” 8:22-35.</p> |
| <p>2. The power converter controller of claim 1, wherein the primary controller is configured to be coupled to a primary side of the power converter, wherein the primary controller is coupled to receive the one or more request signals from a secondary side of the power converter, and wherein the secondary controller</p> | <p>Fig. 4 in Morong shows the primary controller (elements 213d-242d) configured to be coupled to a primary side of the power converter (element 10d), wherein the primary controller is coupled to receive the one or more request signals from a secondary side of the power converter (element 10d), and wherein the secondary controller (elements 400d-509d) is configured to be coupled to the secondary side of the power converter (element 10d).</p> |

EXHIBIT B

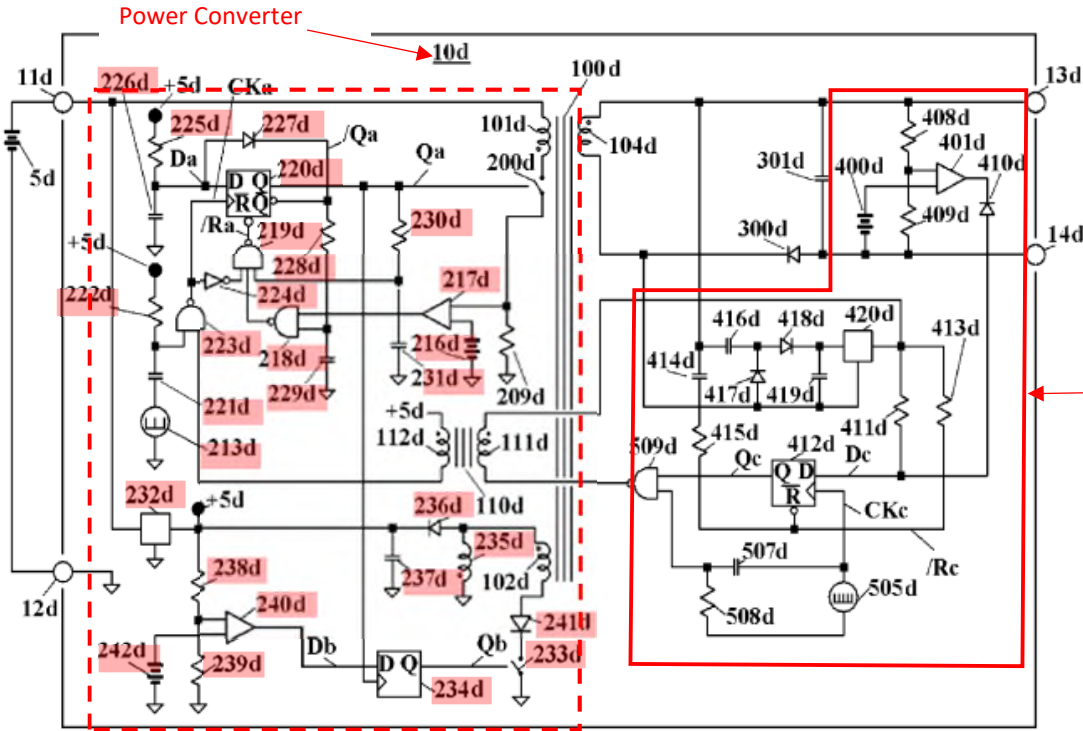
| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|--|--|
| <p>is configured to be coupled to the secondary side of the power converter.</p> |  <p>The diagram illustrates a power converter controller circuit. It is divided into three main functional blocks: a Primary Controller (indicated by a dashed red box), a Power Converter (indicated by a solid red box), and a Secondary Controller (indicated by a solid red box). The Primary Controller includes various logic gates (e.g., 222d, 223d, 224d, 228d, 229d, 232d, 238d, 240d, 242d), flip-flops (220d, 234d), and comparators (217d, 235d). It is connected to a power source (11d, 12d) and a transformer (101d, 102d, 111d, 112d). The Power Converter block contains a bridge rectifier (226d, 227d, 228d, 229d), a filter capacitor (225d), and a switching transistor (Qa). The Secondary Controller block includes a timing circuit (505d, 507d, 508d, 509d), a flip-flop (412d), and a NAND gate (411d). It is connected to the transformer (112d) and a load (13d, 14d). The circuit is labeled with various reference numerals (e.g., 10d, 100d, 101d, 104d, 110d, 12d, 13d, 14d, 200d, 209d, 216d, 217d, 218d, 219d, 220d, 221d, 222d, 223d, 224d, 225d, 226d, 227d, 228d, 229d, 230d, 231d, 232d, 233d, 234d, 235d, 236d, 237d, 238d, 239d, 240d, 241d, 242d, 243d, 244d, 245d, 246d, 247d, 248d, 249d, 250d, 251d, 252d, 253d, 254d, 255d, 256d, 257d, 258d, 259d, 260d, 261d, 262d, 263d, 264d, 265d, 266d, 267d, 268d, 269d, 270d, 271d, 272d, 273d, 274d, 275d, 276d, 277d, 278d, 279d, 280d, 281d, 282d, 283d, 284d, 285d, 286d, 287d, 288d, 289d, 290d, 291d, 292d, 293d, 294d, 295d, 296d, 297d, 298d, 299d, 300d, 301d, 302d, 303d, 304d, 305d, 306d, 307d, 308d, 309d, 310d, 311d, 312d, 313d, 314d, 315d, 316d, 317d, 318d, 319d, 320d, 321d, 322d, 323d, 324d, 325d, 326d, 327d, 328d, 329d, 330d, 331d, 332d, 333d, 334d, 335d, 336d, 337d, 338d, 339d, 340d, 341d, 342d, 343d, 344d, 345d, 346d, 347d, 348d, 349d, 350d, 351d, 352d, 353d, 354d, 355d, 356d, 357d, 358d, 359d, 360d, 361d, 362d, 363d, 364d, 365d, 366d, 367d, 368d, 369d, 370d, 371d, 372d, 373d, 374d, 375d, 376d, 377d, 378d, 379d, 380d, 381d, 382d, 383d, 384d, 385d, 386d, 387d, 388d, 389d, 390d, 391d, 392d, 393d, 394d, 395d, 396d, 397d, 398d, 399d, 400d, 401d, 402d, 403d, 404d, 405d, 406d, 407d, 408d, 409d, 410d, 411d, 412d, 413d, 414d, 415d, 416d, 417d, 418d, 419d, 420d, 421d, 422d, 423d, 424d, 425d, 426d, 427d, 428d, 429d, 430d, 431d, 432d, 433d, 434d, 435d, 436d, 437d, 438d, 439d, 440d, 441d, 442d, 443d, 444d, 445d, 446d, 447d, 448d, 449d, 450d, 451d, 452d, 453d, 454d, 455d, 456d, 457d, 458d, 459d, 460d, 461d, 462d, 463d, 464d, 465d, 466d, 467d, 468d, 469d, 470d, 471d, 472d, 473d, 474d, 475d, 476d, 477d, 478d, 479d, 480d, 481d, 482d, 483d, 484d, 485d, 486d, 487d, 488d, 489d, 490d, 491d, 492d, 493d, 494d, 495d, 496d, 497d, 498d, 499d, 500d, 501d, 502d, 503d, 504d, 505d, 506d, 507d, 508d, 509d, 510d, 511d, 512d, 513d, 514d, 515d, 516d, 517d, 518d, 519d, 520d, 521d, 522d, 523d, 524d, 525d, 526d, 527d, 528d, 529d, 530d, 531d, 532d, 533d, 534d, 535d, 536d, 537d, 538d, 539d, 540d, 541d, 542d, 543d, 544d, 545d, 546d, 547d, 548d, 549d, 550d, 551d, 552d, 553d, 554d, 555d, 556d, 557d, 558d, 559d, 560d, 561d, 562d, 563d, 564d, 565d, 566d, 567d, 568d, 569d, 570d, 571d, 572d, 573d, 574d, 575d, 576d, 577d, 578d, 579d, 580d, 581d, 582d, 583d, 584d, 585d, 586d, 587d, 588d, 589d, 590d, 591d, 592d, 593d, 594d, 595d, 596d, 597d, 598d, 599d, 600d, 601d, 602d, 603d, 604d, 605d, 606d, 607d, 608d, 609d, 610d, 611d, 612d, 613d, 614d, 615d, 616d, 617d, 618d, 619d, 620d, 621d, 622d, 623d, 624d, 625d, 626d, 627d, 628d, 629d, 630d, 631d, 632d, 633d, 634d, 635d, 636d, 637d, 638d, 639d, 640d, 641d, 642d, 643d, 644d, 645d, 646d, 647d, 648d, 649d, 650d, 651d, 652d, 653d, 654d, 655d, 656d, 657d, 658d, 659d, 660d, 661d, 662d, 663d, 664d, 665d, 666d, 667d, 668d, 669d, 670d, 671d, 672d, 673d, 674d, 675d, 676d, 677d, 678d, 679d, 680d, 681d, 682d, 683d, 684d, 685d, 686d, 687d, 688d, 689d, 690d, 691d, 692d, 693d, 694d, 695d, 696d, 697d, 698d, 699d, 700d, 701d, 702d, 703d, 704d, 705d, 706d, 707d, 708d, 709d, 710d, 711d, 712d, 713d, 714d, 715d, 716d, 717d, 718d, 719d, 720d, 721d, 722d, 723d, 724d, 725d, 726d, 727d, 728d, 729d, 730d, 731d, 732d, 733d, 734d, 735d, 736d, 737d, 738d, 739d, 740d, 741d, 742d, 743d, 744d, 745d, 746d, 747d, 748d, 749d, 750d, 751d, 752d, 753d, 754d, 755d, 756d, 757d, 758d, 759d, 760d, 761d, 762d, 763d, 764d, 765d, 766d, 767d, 768d, 769d, 770d, 771d, 772d, 773d, 774d, 775d, 776d, 777d, 778d, 779d, 780d, 781d, 782d, 783d, 784d, 785d, 786d, 787d, 788d, 789d, 790d, 791d, 792d, 793d, 794d, 795d, 796d, 797d, 798d, 799d, 800d, 801d, 802d, 803d, 804d, 805d, 806d, 807d, 808d, 809d, 810d, 811d, 812d, 813d, 814d, 815d, 816d, 817d, 818d, 819d, 820d, 821d, 822d, 823d, 824d, 825d, 826d, 827d, 828d, 829d, 830d, 831d, 832d, 833d, 834d, 835d, 836d, 837d, 838d, 839d, 840d, 841d, 842d, 843d, 844d, 845d, 846d, 847d, 848d, 849d, 850d, 851d, 852d, 853d, 854d, 855d, 856d, 857d, 858d, 859d, 860d, 861d, 862d, 863d, 864d, 865d, 866d, 867d, 868d, 869d, 870d, 871d, 872d, 873d, 874d, 875d, 876d, 877d, 878d, 879d, 880d, 881d, 882d, 883d, 884d, 885d, 886d, 887d, 888d, 889d, 890d, 891d, 892d, 893d, 894d, 895d, 896d, 897d, 898d, 899d, 900d, 901d, 902d, 903d, 904d, 905d, 906d, 907d, 908d, 909d, 910d, 911d, 912d, 913d, 914d, 915d, 916d, 917d, 918d, 919d, 920d, 921d, 922d, 923d, 924d, 925d, 926d, 927d, 928d, 929d, 930d, 931d, 932d, 933d, 934d, 935d, 936d, 937d, 938d, 939d, 940d, 941d, 942d, 943d, 944d, 945d, 946d, 947d, 948d, 949d, 950d, 951d, 952d, 953d, 954d, 955d, 956d, 957d, 958d, 959d, 960d, 961d, 962d, 963d, 964d, 965d, 966d, 967d, 968d, 969d, 970d, 971d, 972d, 973d, 974d, 975d, 976d, 977d, 978d, 979d, 980d, 981d, 982d, 983d, 984d, 985d, 986d, 987d, 988d, 989d, 990d, 991d, 992d, 993d, 994d, 995d, 996d, 997d, 998d, 999d, 1000d).</p> |
| <p>3. The power converter controller of claim 1, wherein the secondary controller includes a timing circuit that sets a minimum amount of time</p> | <p>Fig. 4 in Morong shows a power converter controller wherein the secondary controller (elements 400d-509d) includes a timing circuit (at least oscillator 505d + flip-flop 412d) that sets a minimum amount of time between the transmission of each of the one or more request signals. <i>See also</i> 7:50-52 (“These winding 112d pulses are conveyed through a NAND gate 223d to clock flip-flop 220d at up to the frequency of oscillator 505d.”).</p> |

EXHIBIT B

| | |
|---|--|
| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
| <p>between the transmission of each of the one or more request signals.</p> | <p>The diagram shows a complex electronic circuit for a power converter controller. It includes a primary controller section (left) with components like 11d, 5d, 226d, 225d, 227d, 220d, 219d, 228d, 224d, 223d, 221d, 213d, 232d, 238d, 240d, 242d, 239d, 237d, 235d, 241d, 233d, 234d, 236d, 110d, 102d, 101d, 200d, 104d, 100d, 13d, 14d, 103d, 105d, 106d, 107d, 108d, 109d, 111d, 112d, 113d, 114d, 115d, 116d, 117d, 118d, 119d, 120d, 121d, 122d, 123d, 124d, 125d, 126d, 127d, 128d, 129d, 130d, 131d, 132d, 133d, 134d, 135d, 136d, 137d, 138d, 139d, 140d, 141d, 142d, 143d, 144d, 145d, 146d, 147d, 148d, 149d, 150d, 151d, 152d, 153d, 154d, 155d, 156d, 157d, 158d, 159d, 160d, 161d, 162d, 163d, 164d, 165d, 166d, 167d, 168d, 169d, 170d, 171d, 172d, 173d, 174d, 175d, 176d, 177d, 178d, 179d, 180d, 181d, 182d, 183d, 184d, 185d, 186d, 187d, 188d, 189d, 190d, 191d, 192d, 193d, 194d, 195d, 196d, 197d, 198d, 199d, 200d, 201d, 202d, 203d, 204d, 205d, 206d, 207d, 208d, 209d, 210d, 211d, 212d, 213d, 214d, 215d, 216d, 217d, 218d, 219d, 220d, 221d, 222d, 223d, 224d, 225d, 226d, 227d, 228d, 229d, 230d, 231d, 232d, 233d, 234d, 235d, 236d, 237d, 238d, 239d, 240d, 241d, 242d, 243d, 244d, 245d, 246d, 247d, 248d, 249d, 250d, 251d, 252d, 253d, 254d, 255d, 256d, 257d, 258d, 259d, 260d, 261d, 262d, 263d, 264d, 265d, 266d, 267d, 268d, 269d, 270d, 271d, 272d, 273d, 274d, 275d, 276d, 277d, 278d, 279d, 280d, 281d, 282d, 283d, 284d, 285d, 286d, 287d, 288d, 289d, 290d, 291d, 292d, 293d, 294d, 295d, 296d, 297d, 298d, 299d, 300d, 301d, 302d, 303d, 304d, 305d, 306d, 307d, 308d, 309d, 310d, 311d, 312d, 313d, 314d, 315d, 316d, 317d, 318d, 319d, 320d, 321d, 322d, 323d, 324d, 325d, 326d, 327d, 328d, 329d, 330d, 331d, 332d, 333d, 334d, 335d, 336d, 337d, 338d, 339d, 340d, 341d, 342d, 343d, 344d, 345d, 346d, 347d, 348d, 349d, 350d, 351d, 352d, 353d, 354d, 355d, 356d, 357d, 358d, 359d, 360d, 361d, 362d, 363d, 364d, 365d, 366d, 367d, 368d, 369d, 370d, 371d, 372d, 373d, 374d, 375d, 376d, 377d, 378d, 379d, 380d, 381d, 382d, 383d, 384d, 385d, 386d, 387d, 388d, 389d, 390d, 391d, 392d, 393d, 394d, 395d, 396d, 397d, 398d, 399d, 400d, 401d, 402d, 403d, 404d, 405d, 406d, 407d, 408d, 409d, 410d, 411d, 412d, 413d, 414d, 415d, 416d, 417d, 418d, 419d, 420d, 421d, 422d, 423d, 424d, 425d, 426d, 427d, 428d, 429d, 430d, 431d, 432d, 433d, 434d, 435d, 436d, 437d, 438d, 439d, 440d, 441d, 442d, 443d, 444d, 445d, 446d, 447d, 448d, 449d, 450d, 451d, 452d, 453d, 454d, 455d, 456d, 457d, 458d, 459d, 460d, 461d, 462d, 463d, 464d, 465d, 466d, 467d, 468d, 469d, 470d, 471d, 472d, 473d, 474d, 475d, 476d, 477d, 478d, 479d, 480d, 481d, 482d, 483d, 484d, 485d, 486d, 487d, 488d, 489d, 490d, 491d, 492d, 493d, 494d, 495d, 496d, 497d, 498d, 499d, 500d, 501d, 502d, 503d, 504d, 505d, 506d, 507d, 508d, 509d, 510d, 511d, 512d, 513d, 514d, 515d, 516d, 517d, 518d, 519d, 520d, 521d, 522d, 523d, 524d, 525d, 526d, 527d, 528d, 529d, 530d, 531d, 532d, 533d, 534d, 535d, 536d, 537d, 538d, 539d, 540d, 541d, 542d, 543d, 544d, 545d, 546d, 547d, 548d, 549d, 550d, 551d, 552d, 553d, 554d, 555d, 556d, 557d, 558d, 559d, 560d, 561d, 562d, 563d, 564d, 565d, 566d, 567d, 568d, 569d, 570d, 571d, 572d, 573d, 574d, 575d, 576d, 577d, 578d, 579d, 580d, 581d, 582d, 583d, 584d, 585d, 586d, 587d, 588d, 589d, 590d, 591d, 592d, 593d, 594d, 595d, 596d, 597d, 598d, 599d, 600d, 601d, 602d, 603d, 604d, 605d, 606d, 607d, 608d, 609d, 610d, 611d, 612d, 613d, 614d, 615d, 616d, 617d, 618d, 619d, 620d, 621d, 622d, 623d, 624d, 625d, 626d, 627d, 628d, 629d, 630d, 631d, 632d, 633d, 634d, 635d, 636d, 637d, 638d, 639d, 640d, 641d, 642d, 643d, 644d, 645d, 646d, 647d, 648d, 649d, 650d, 651d, 652d, 653d, 654d, 655d, 656d, 657d, 658d, 659d, 660d, 661d, 662d, 663d, 664d, 665d, 666d, 667d, 668d, 669d, 670d, 671d, 672d, 673d, 674d, 675d, 676d, 677d, 678d, 679d, 680d, 681d, 682d, 683d, 684d, 685d, 686d, 687d, 688d, 689d, 690d, 691d, 692d, 693d, 694d, 695d, 696d, 697d, 698d, 699d, 700d, 701d, 702d, 703d, 704d, 705d, 706d, 707d, 708d, 709d, 710d</p> |

EXHIBIT B

| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|---|--|
| <p>power switch while the power switch is in the ON state;</p> | <p style="text-align: center;">Fig. 4</p> |
| <p>determine when the amount of current through the power switch is greater than the threshold current limit; and</p> | <p>Fig. 4 of Morong shows power converter controller wherein the primary controller (elements 213d-242d) is coupled to determine when the amount of current through the power switch (switch 200d) is greater than the threshold current limit (value set by reference 216d). See 7:1-5 (“When current in resistor 209d exceeds a value set by reference 216d, comparator 217d issues a reset signal which propagates through NAND gates 218d and 219d to a node /Ra where the reset signal resets flip-flop 220d, turning OFF switch 200d.”).</p> |

EXHIBIT B

U.S. Pat. No. 9,166,486

U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian)

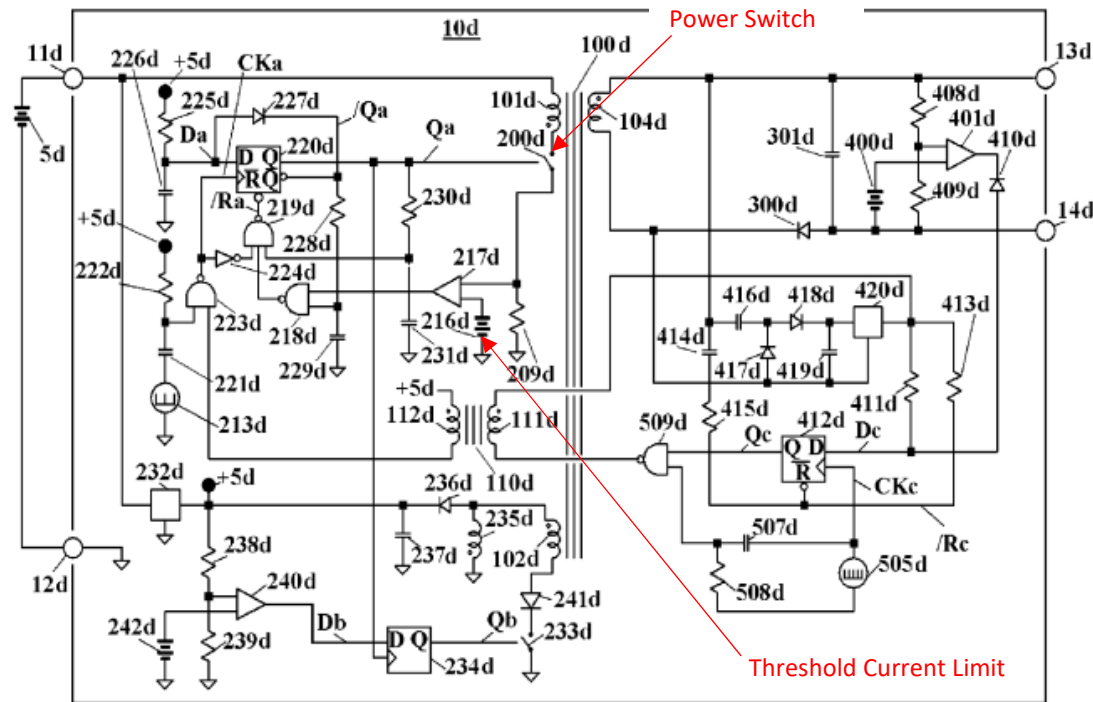


Fig. 4

transition the power switch from the ON state to the OFF state when the amount of current through the power switch

Fig. 4 of Morong shows power converter controller wherein the primary controller (elements 213d-242d) is coupled to transition the power switch (switch 200d) from the ON state to the OFF state when the amount of current through the power switch (switch 200d) is greater than the threshold current limit (value set by reference 216d). See 7:1-5 (“When current in resistor 209d exceeds a value set by reference 216d,

EXHIBIT B

| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|---|--|
| is greater than the threshold current limit. | comparator 217d issues a reset signal which propagates through NAND gates 218d and 219d to a node /Ra where the reset signal resets flip-flop 220d, turning OFF switch 200d.”). |
| 6. The power converter controller of claim 1, wherein the secondary controller is coupled to transmit the request signals via a communication link, wherein the primary controller is coupled to receive the request signals via the communication link, and wherein the communication link includes at least one of an optical communication link, a capacitive communication link, and a magnetic communication link. | Fig. 4 of Morong shows a power converter controller wherein the secondary controller (elements 400d-509d) is coupled to transmit the request signals (demand pulses) via a communication link (demand pulse transformer 110d), wherein the primary controller (elements 213d-242d) is coupled to receive the request signals via the communication link, and wherein the communication link includes at least one of an optical communication link, a capacitive communication link, and a magnetic communication link. <i>See</i> 9:4-6 (“The converter may comprise inductive, capacitive, opto-coupled, or piezoelectric galvanic isolation circuitry to transmit demand pulses across the galvanic isolation barrier.”). |

EXHIBIT B

| | |
|--|--|
| <p>U.S. Pat. No. 9,166,486</p> | <p>U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian)</p> |
| | <p>Fig. 4</p> <p>Primary Controller</p> <p>Secondary Controller</p> <p>Communication Link</p> |
| <p>7. The power converter controller of claim 3, wherein the minimum amount of time between the transmission of each of the one or more request signals sets a minimum amount of time between two consecutive transitions of the power switch from the OFF state to the ON state. <i>See</i> 7:50-52 (“These winding 112d pulses are conveyed through a NAND gate 223d to clock flip-flop 220d at up to the frequency of oscillator 505d.”).</p> | <p>Fig. 4 of Morong shows a power converter controller wherein the minimum amount of time between the transmission of each of the one or more request signals sets a minimum amount of time between two consecutive transitions of the power switch from the OFF state to the ON state. <i>See</i> 7:50-52 (“These winding 112d pulses are conveyed through a NAND gate 223d to clock flip-flop 220d at up to the frequency of oscillator 505d.”).</p> |

EXHBIT B

| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|---|--|
| request signals sets a minimum amount of time between two consecutive transitions of the power switch from the OFF state to the ON state. | |
| 8. The power converter controller of claim 3, wherein the timing circuit is coupled to operate in a first state until triggered to operate in a second state, wherein the timing circuit is in the second state for a holding period and transitions back to the first state at an end of the holding period, and wherein the holding period sets the minimum amount of time between the transmission of two consecutive request signals. | Fig. 4 of Morong shows a power converter controller wherein the timing circuit (at least oscillator 505d + flip-flop 412d) is coupled to operate in a first state (rising edge of clock signal at node CKc from oscillator 505d) until triggered to operate in a second state (duration between consecutive rising edges of clock signal at node CKc from oscillator 505d), wherein the timing circuit is in the second state for a holding period and transitions back to the first state at an end of the holding period, and wherein the holding period sets the minimum amount of time between the transmission of two consecutive request signals. <i>See</i> 7:50-61 (“These winding 112 <i>d</i> pulses are conveyed through a NAND gate 223 <i>d</i> to clock flip-flop 220 <i>d</i> at up to the frequency of oscillator 505 <i>d</i> . If all of the pulses of oscillator 505 <i>d</i> were allowed to clock flip-flop 220 <i>d</i> , under some conditions, the converter of this embodiment would produce excess output. To regulate this output, a flip-flop 412 <i>d</i> is used to gate the pulses passed by NAND gate 509 <i>d</i> . At a node CKc, oscillator 505 <i>d</i> clocks a flip-flop 412 <i>d</i> , which generates a logic high at a node Qc only when a logic high is present at a node Dc at the rising edge of its clock. Thus, pulses driving transformer 110 <i>d</i> are permitted responsive to a logic high only at node Dc.”). |
| 9. The power converter controller of claim 8, wherein the secondary | Fig. 4 of Morong shows a power converter controller wherein the secondary controller (elements 400d-509d) includes a secondary switch control circuit (at least elements 401d, 410d, 412d, 509d) coupled to sense an output quantity (voltage at terminals 13d and 14d) of the power converter (10d) and transmit one |

EXHBIT B

| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|--|--|
| <p>controller includes a secondary switch control circuit coupled to sense an output quantity of the power converter and transmit one of the request signals to the primary controller when the a sensed output quantity is less than a desired output quantity and the timing circuit is in the first state, wherein the secondary switch control circuit triggers the timing circuit in response to transmitting the request signal.</p> | <p>of the request signals (demand pulses) to the primary controller (elements 213d-242d) when the sensed output quantity is less than a desired output quantity (proportional to voltage of reference 400d) and the timing circuit (oscillator 505d + flip-flop 412d) is in the first state (rising edge of clock signal at node CKc from oscillator 505d), wherein the secondary switch control circuit triggers the timing circuit in response to transmitting the request signal. <i>See</i> 8:6-19 (“Node Dc is usually held at a logic high by a resistor 411d, thus enabling pulses gated by flip-flop 412d. However, between terminals 13d and 14d is disposed a voltage divider comprising resistors 408d and 409d, the voltage at the junction of which is applied to an input of a comparator 401d. Should the voltage at that junction exceed the voltage of a reference 400d, also applied to a comparator 401d input, an output of comparator 401d will drop to a logic low, drawing current through a diode 410d, thus presenting a logic low at node Dc and, after clocking, responsively at node Qc, inhibiting pulses through gate 509d that would otherwise turn ON switch 200d. Thus, the voltage between terminals 13d and 14d is regulated responsive to the voltage of reference 400d.”). To the extent that Power Integrations argues that Fig. 4 of Morong does not expressly show a secondary switch control circuit that triggers the timing circuit in response to transmitting the request signal, it would have be obvious to a person of ordinary skill in the art to implement a power converter having this feature based on the teachings in at least Morong and Djenguerian.</p> |

EXHIBIT B

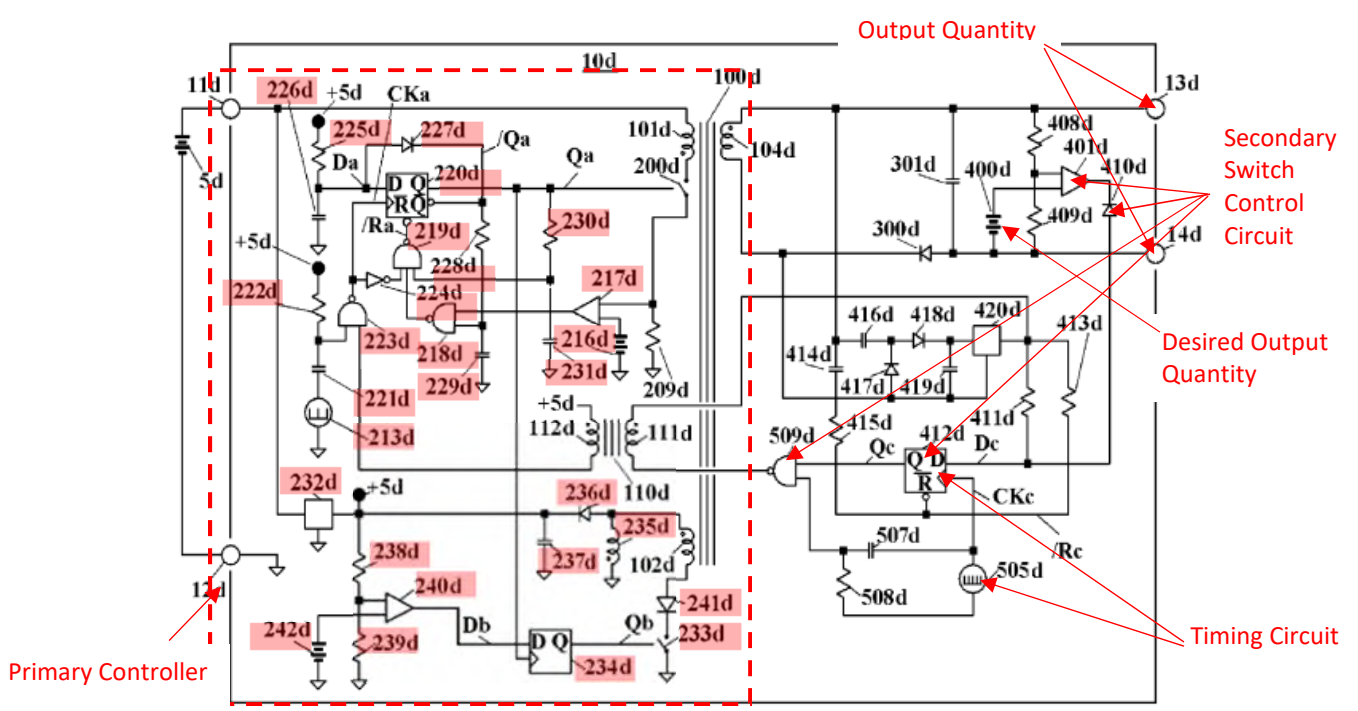
| | |
|---|---|
| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
| <p>11. A power converter controller comprising:</p> |  <p>The diagram illustrates a power converter controller circuit. It is divided into several functional blocks:</p> <ul style="list-style-type: none"> Primary Controller (213d-242d): This block, enclosed in a dashed red box, contains the main control logic. It includes a power MOSFET (226d) driven by a gate driver (225d, 227d, 228d, 229d). The MOSFET is connected to a transformer (101d, 102d) which provides isolation and voltage transformation. The primary controller also includes a feedback network (222d, 223d, 224d, 232d, 233d, 234d, 235d, 236d, 237d, 238d, 239d, 240d, 241d, 242d) and a timing network (216d, 217d, 218d, 219d, 220d, 221d, 222d, 223d, 224d, 225d, 226d, 227d, 228d, 229d, 230d, 231d, 232d, 233d, 234d, 235d, 236d, 237d, 238d, 239d, 240d, 241d, 242d). Secondary Switch Control Circuit (400d-409d): This circuit, also in a dashed red box, provides a secondary switching function. It includes a MOSFET (408d) and a diode (409d) connected to a transformer (104d). Timing Circuit (410d-419d): This circuit, in a dashed red box, generates precise timing signals for the converter. It includes a MOSFET (416d) and a diode (417d) connected to a transformer (104d). Output Quantity (13d, 14d): This block measures the output quantity of the converter. It includes a transformer (104d) and a diode (409d) connected to a transformer (104d). <p>The circuit is powered by a 5d supply and includes various passive components like resistors (101d, 102d, 104d, 105d, 106d, 107d, 108d, 109d, 110d, 111d, 112d, 113d, 114d, 115d, 116d, 117d, 118d, 119d, 120d, 121d, 122d, 123d, 124d, 125d, 126d, 127d, 128d, 129d, 130d, 131d, 132d, 133d, 134d, 135d, 136d, 137d, 138d, 139d, 140d, 141d, 142d, 143d, 144d, 145d, 146d, 147d, 148d, 149d, 150d, 151d, 152d, 153d, 154d, 155d, 156d, 157d, 158d, 159d, 160d, 161d, 162d, 163d, 164d, 165d, 166d, 167d, 168d, 169d, 170d, 171d, 172d, 173d, 174d, 175d, 176d, 177d, 178d, 179d, 180d, 181d, 182d, 183d, 184d, 185d, 186d, 187d, 188d, 189d, 190d, 191d, 192d, 193d, 194d, 195d, 196d, 197d, 198d, 199d, 200d, 201d, 202d, 203d, 204d, 205d, 206d, 207d, 208d, 209d, 210d, 211d, 212d, 213d, 214d, 215d, 216d, 217d, 218d, 219d, 220d, 221d, 222d, 223d, 224d, 225d, 226d, 227d, 228d, 229d, 230d, 231d, 232d, 233d, 234d, 235d, 236d, 237d, 238d, 239d, 240d, 241d, 242d, 243d, 244d, 245d, 246d, 247d, 248d, 249d, 250d, 251d, 252d, 253d, 254d, 255d, 256d, 257d, 258d, 259d, 260d, 261d, 262d, 263d, 264d, 265d, 266d, 267d, 268d, 269d, 270d, 271d, 272d, 273d, 274d, 275d, 276d, 277d, 278d, 279d, 280d, 281d, 282d, 283d, 284d, 285d, 286d, 287d, 288d, 289d, 290d, 291d, 292d, 293d, 294d, 295d, 296d, 297d, 298d, 299d, 300d, 301d, 302d, 303d, 304d, 305d, 306d, 307d, 308d, 309d, 310d, 311d, 312d, 313d, 314d, 315d, 316d, 317d, 318d, 319d, 320d, 321d, 322d, 323d, 324d, 325d, 326d, 327d, 328d, 329d, 330d, 331d, 332d, 333d, 334d, 335d, 336d, 337d, 338d, 339d, 340d, 341d, 342d, 343d, 344d, 345d, 346d, 347d, 348d, 349d, 350d, 351d, 352d, 353d, 354d, 355d, 356d, 357d, 358d, 359d, 360d, 361d, 362d, 363d, 364d, 365d, 366d, 367d, 368d, 369d, 370d, 371d, 372d, 373d, 374d, 375d, 376d, 377d, 378d, 379d, 380d, 381d, 382d, 383d, 384d, 385d, 386d, 387d, 388d, 389d, 390d, 391d, 392d, 393d, 394d, 395d, 396d, 397d, 398d, 399d, 400d, 401d, 402d, 403d, 404d, 405d, 406d, 407d, 408d, 409d, 410d, 411d, 412d, 413d, 414d, 415d, 416d, 417d, 418d, 419d, 420d, 421d, 422d, 423d, 424d, 425d, 426d, 427d, 428d, 429d, 430d, 431d, 432d, 433d, 434d, 435d, 436d, 437d, 438d, 439d, 440d, 441d, 442d, 443d, 444d, 445d, 446d, 447d, 448d, 449d, 450d, 451d, 452d, 453d, 454d, 455d, 456d, 457d, 458d, 459d, 460d, 461d, 462d, 463d, 464d, 465d, 466d, 467d, 468d, 469d, 470d, 471d, 472d, 473d, 474d, 475d, 476d, 477d, 478d, 479d, 480d, 481d, 482d, 483d, 484d, 485d, 486d, 487d, 488d, 489d, 490d, 491d, 492d, 493d, 494d, 495d, 496d, 497d, 498d, 499d, 500d, 501d, 502d, 503d, 504d, 505d, 506d, 507d, 508d, 509d, 510d, 511d, 512d, 513d, 514d, 515d, 516d, 517d, 518d, 519d, 520d, 521d, 522d, 523d, 524d, 525d, 526d, 527d, 528d, 529d, 530d, 531d, 532d, 533d, 534d, 535d, 536d, 537d, 538d, 539d, 540d, 541d, 542d, 543d, 544d, 545d, 546d, 547d, 548d, 549d, 550d, 551d, 552d, 553d, 554d, 555d, 556d, 557d, 558d, 559d, 560d, 561d, 562d, 563d, 564d, 565d, 566d, 567d, 568d, 569d, 570d, 571d, 572d, 573d, 574d, 575d, 576d, 577d, 578d, 579d, 580d, 581d, 582d, 583d, 584d, 585d, 586d, 587d, 588d, 589d, 590d, 591d, 592d, 593d, 594d, 595d, 596d, 597d, 598d, 599d, 600d, 601d, 602d, 603d, 604d, 605d, 606d, 607d, 608d, 609d, 610d, 611d, 612d, 613d, 614d, 615d, 616d, 617d, 618d, 619d, 620d, 621d, 622d, 623d, 624d, 625d, 626d, 627d, 628d, 629d, 630d, 631d, 632d, 633d, 634d, 635d, 636d, 637d, 638d, 639d, 640d, 641d, </p> |

EXHIBIT B

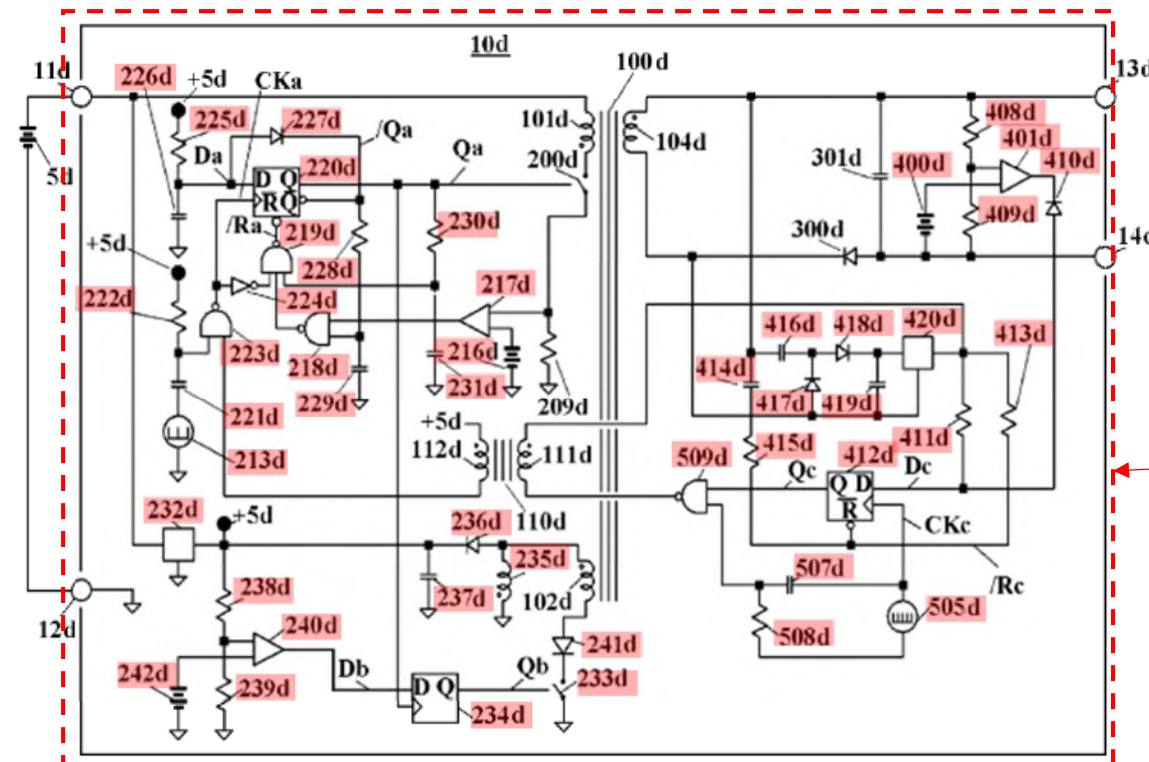
| | |
|--------------------------------|---|
| <p>U.S. Pat. No. 9,166,486</p> | <p>U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian)</p> |
| |  <p>The diagram illustrates a complex electronic circuit, identified as a secondary controller. It features a central transformer with multiple windings (101d, 102d, 103d, 104d, 105d, 106d, 107d, 108d, 109d, 110d, 111d, 112d, 113d, 114d, 115d, 116d, 117d, 118d, 119d, 120d, 121d, 122d, 123d, 124d, 125d, 126d, 127d, 128d, 129d, 130d, 131d, 132d, 133d, 134d, 135d, 136d, 137d, 138d, 139d, 140d, 141d, 142d, 143d, 144d, 145d, 146d, 147d, 148d, 149d, 150d, 151d, 152d, 153d, 154d, 155d, 156d, 157d, 158d, 159d, 160d, 161d, 162d, 163d, 164d, 165d, 166d, 167d, 168d, 169d, 170d, 171d, 172d, 173d, 174d, 175d, 176d, 177d, 178d, 179d, 180d, 181d, 182d, 183d, 184d, 185d, 186d, 187d, 188d, 189d, 190d, 191d, 192d, 193d, 194d, 195d, 196d, 197d, 198d, 199d, 200d, 201d, 202d, 203d, 204d, 205d, 206d, 207d, 208d, 209d, 210d, 211d, 212d, 213d, 214d, 215d, 216d, 217d, 218d, 219d, 220d, 221d, 222d, 223d, 224d, 225d, 226d, 227d, 228d, 229d, 230d, 231d, 232d, 233d, 234d, 235d, 236d, 237d, 238d, 239d, 240d, 241d, 242d, 243d, 244d, 245d, 246d, 247d, 248d, 249d, 250d, 251d, 252d, 253d, 254d, 255d, 256d, 257d, 258d, 259d, 260d, 261d, 262d, 263d, 264d, 265d, 266d, 267d, 268d, 269d, 270d, 271d, 272d, 273d, 274d, 275d, 276d, 277d, 278d, 279d, 280d, 281d, 282d, 283d, 284d, 285d, 286d, 287d, 288d, 289d, 290d, 291d, 292d, 293d, 294d, 295d, 296d, 297d, 298d, 299d, 300d, 301d, 302d, 303d, 304d, 305d, 306d, 307d, 308d, 309d, 310d, 311d, 312d, 313d, 314d, 315d, 316d, 317d, 318d, 319d, 320d, 321d, 322d, 323d, 324d, 325d, 326d, 327d, 328d, 329d, 330d, 331d, 332d, 333d, 334d, 335d, 336d, 337d, 338d, 339d, 340d, 341d, 342d, 343d, 344d, 345d, 346d, 347d, 348d, 349d, 350d, 351d, 352d, 353d, 354d, 355d, 356d, 357d, 358d, 359d, 360d, 361d, 362d, 363d, 364d, 365d, 366d, 367d, 368d, 369d, 370d, 371d, 372d, 373d, 374d, 375d, 376d, 377d, 378d, 379d, 380d, 381d, 382d, 383d, 384d, 385d, 386d, 387d, 388d, 389d, 390d, 391d, 392d, 393d, 394d, 395d, 396d, 397d, 398d, 399d, 400d, 401d, 402d, 403d, 404d, 405d, 406d, 407d, 408d, 409d, 410d, 411d, 412d, 413d, 414d, 415d, 416d, 417d, 418d, 419d, 420d, 421d, 422d, 423d, 424d, 425d, 426d, 427d, 428d, 429d, 430d, 431d, 432d, 433d, 434d, 435d, 436d, 437d, 438d, 439d, 440d, 441d, 442d, 443d, 444d, 445d, 446d, 447d, 448d, 449d, 450d, 451d, 452d, 453d, 454d, 455d, 456d, 457d, 458d, 459d, 460d, 461d, 462d, 463d, 464d, 465d, 466d, 467d, 468d, 469d, 470d, 471d, 472d, 473d, 474d, 475d, 476d, 477d, 478d, 479d, 480d, 481d, 482d, 483d, 484d, 485d, 486d, 487d, 488d, 489d, 490d, 491d, 492d, 493d, 494d, 495d, 496d, 497d, 498d, 499d, 500d, 501d, 502d, 503d, 504d, 505d, 506d, 507d, 508d, 509d, 510d, 511d, 512d, 513d, 514d, 515d, 516d, 517d, 518d, 519d, 520d, 521d, 522d, 523d, 524d, 525d, 526d, 527d, 528d, 529d, 530d, 531d, 532d, 533d, 534d, 535d, 536d, 537d, 538d, 539d, 540d, 541d, 542d, 543d, 544d, 545d, 546d, 547d, 548d, 549d, 550d, 551d, 552d, 553d, 554d, 555d, 556d, 557d, 558d, 559d, 560d, 561d, 562d, 563d, 564d, 565d, 566d, 567d, 568d, 569d, 570d, 571d, 572d, 573d, 574d, 575d, 576d, 577d, 578d, 579d, 580d, 581d, 582d, 583d, 584d, 585d, 586d, 587d, 588d, 589d, 590d, 591d, 592d, 593d, 594d, 595d, 596d, 597d, 598d, 599d, 600d, 601d, 602d, 603d, 604d, 605d, 606d, 607d, 608d, 609d, 610d, 611d, 612d, 613d, 614d, 615d, 616d, 617d, 618d, 619d, 620d, 621d, 622d, 623d, 624d, 625d, 626d, 627d, 628d, 629d, 630d, 631d, 632d, 633d, 634d, 635d, 636d, 637d, 638d, 639d, 640d, 641d, 642d, 643d, 644d, 645d, 646d, 647d, 648d, 649d, 650d, 651d, 652d, 653d, 654d, 655d, 656d, 657d, 658d, 659d, 660d, 661d, 662d, 663d, 664d, 665d, 666d, 667d, 668d, 669d, 670d, 671d, 672d, 673d, 674d, 675d, 676d, 677d, 678d, 679d, 680d, 681d, 682d, 683d, 684d, 685d, 686d, 687d, 688d, 689d, 690d, 691d, 692d, 693d, 694d, 695d, 696d, 697d, 698d, 699d, 700d, 701d, 702d, 703d, 704d, 705d, 706d, 707d, 708d, 709d, 710d, 711d, 712d, 713d, 714d, 715d, 716d, 717d, 718d, 719d, 720d, 721d, 722d, 723d, 724d, 725d, 726d, 727d, 728d, 729d, 730d, 731d, 732d, 733d, 734d, 735d, 73</p> |

EXHIBIT B

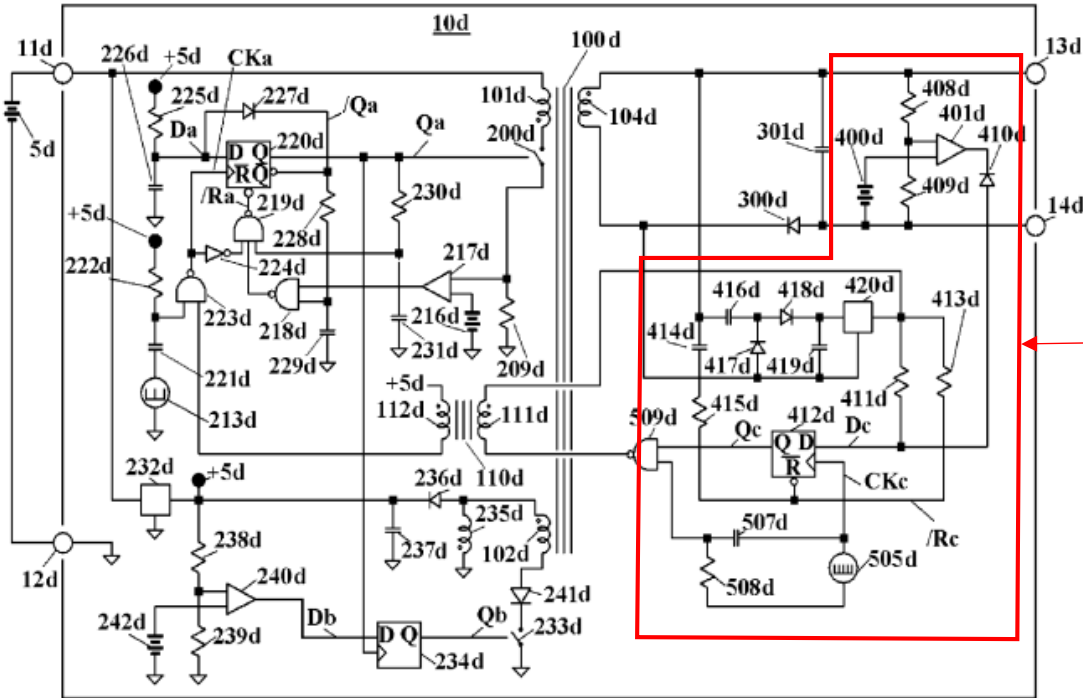
| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|--|--|
| |  <p data-bbox="1073 1036 1213 1092">Fig. 4</p> |
| <p>a timing circuit coupled to operate in a first state until triggered to operate in a second state, wherein the timing circuit is in the</p> | <p>Fig. 4 in Morong shows a secondary controller comprising a timing circuit (at least oscillator 505d + flip-flop 412d) coupled to operate in a first state (rising edge of clock signal at node CKc from oscillator 505d) until triggered to operate in a second state (duration between consecutive rising edges of clock signal at node CKc from oscillator 505d), wherein the timing circuit is in the second state for a holding period and transitions back to the first state at an end of the holding period. <i>See</i> 7:50-61 (“These winding 112 d pulses</p> |

EXHIBIT B

| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|--|--|
| <p>second state for a holding period and transitions back to the first state at an end of the holding period; and</p> | <p>are conveyed through a NAND gate 223 d to clock flip-flop 220 d at up to the frequency of oscillator 505 d. If all of the pulses of oscillator 505 d were allowed to clock flip-flop 220 d, under some conditions, the converter of this embodiment would produce excess output. To regulate this output, a flip-flop 412 d is used to gate the pulses passed by NAND gate 509 d. At a node CKc, oscillator 505 d clocks a flip-flop 412 d, which generates a logic high at a node Qc only when a logic high is present at a node Dc at the rising edge of its clock. Thus, pulses driving transformer 110 d are permitted responsive to a logic high only at node Dc.”).</p> |
| <p>a secondary switch control circuit coupled to sense an output quantity of a power converter and transmit a request signal when the a sensed output quantity is less than a desired output quantity and the timing circuit is in the first state, wherein the secondary switch control circuit triggers the timing circuit in response to transmitting the request signal; and</p> | <p>Fig. 4 in Morong shows a secondary controller comprising a secondary switch control circuit (comparator 401d) coupled to sense an output quantity (voltage at terminals 13d and 14d) of a power converter and transmit a request signal when the a sensed output quantity is less than a desired output quantity (proportional to voltage of reference 400d) and the timing circuit (at least oscillator 505d + flip-flop 412d) is in the first state, wherein the secondary switch control circuit triggers the timing circuit in response to transmitting the request signal. <i>See</i> 8:6-19 (“Node Dc is usually held at a logic high by a resistor 411d, thus enabling pulses gated by flip-flop 412d. However, between terminals 13d and 14d is disposed a voltage divider comprising resistors 408d and 409d, the voltage at the junction of which is applied to an input of a comparator 401d. Should the voltage at that junction exceed the voltage of a reference 400d, also applied to a comparator 401d input, an output of comparator 401d will drop to a logic low, drawing current through a diode 410d, thus presenting a logic low at node Dc and, after clocking, responsively at node Qc, inhibiting pulses through gate 509d that would otherwise turn ON switch 200d. Thus, the voltage between terminals 13d and 14d is regulated responsive to the voltage of reference 400d.”). To the extent that Power Integrations argues that Fig. 4 of Morong does not expressly show a secondary switch control circuit that triggers the timing circuit in response to transmitting the request signal, it would have been obvious to a person of ordinary skill in the art to implement a power converter having this feature based on the teachings in at least Morong and Djenguerian.</p> |

EXHIBIT B

| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|---|--|
| <p>a primary controller to be coupled to a power switch of the power converter and galvanically isolated from the secondary controller, wherein the primary controller is coupled to receive the transmitted request signal and set the power switch into an ON state in response to the request signal, and wherein the primary controller is coupled to detect a turn-off condition and transition the power switch from the ON state to an OFF state in response to detection of the turn-off condition,</p> | <p>Fig. 4 in Morong shows a primary controller (elements 213d-242d) to be coupled to a power switch (switch 200d) of the power converter (10d) and galvanically isolated from the secondary controller (elements 400d-509d),</p> <p>wherein the primary controller is coupled to receive the transmitted request signal (demand pulse) and set the power switch into an ON state in response to the request signal (7:42-61 “The ON pulses of switch 200d responsive to oscillator 213d are sufficiently frequent to start the converter of this embodiment, but insufficiently frequent to drive it to full output. To initiate more frequent pulses, an oscillator 505d drives a capacitor 507d and a resistor 508d to supply differentiated pulses of about 100 nS width to a NAND gate 509d, which in turn drives a primary winding 111d of demand pulse transformer 110d, thus producing demand pulses across a secondary winding 112d thereof. These winding 112d pulses are conveyed through a NAND gate 223d to clock flip-flop 220d at up to the frequency of oscillator 505d. If all of the pulses of oscillator 505d were allowed to clock flip-flop 220d, under some conditions, the converter of this embodiment would produce excess output. To regulate this output, a flip-flop 412d is used to gate the pulses passed by NAND gate 509d. At a node CKc, oscillator 505d clocks a flip-flop 412d, which generates a logic high at a node Qc only when a logic high is present at a node Dc at the rising edge of its clock. Thus, pulses driving transformer 110d are permitted responsive to a logic high only at node Dc.”),</p> <p>and wherein the primary controller is coupled to detect a turn-off condition and transition the power switch (switch 200d) from the ON state to an OFF state in response to detection of the turn-off condition (7:1-5 “When current in resistor 209d exceeds a value set by reference 216d, comparator 217d issues a reset signal which propagates through NAND gates 218d and 219d to a node /Ra where the reset signal resets flip-flop 220d, turning OFF switch 200d.”).</p> |
| <p>wherein the primary controller is configured to maintain the power switch in the OFF state for a threshold period of</p> | <p>Fig. 4 in Morong shows a primary controller (elements 213d-242d) configured to maintain the power switch (switch 200d) in the OFF state for a threshold period of time after transitioning the power switch to the OFF state, and wherein the primary controller is configured to refrain from setting the power switch into the ON state in response to a subsequent request signal received during the threshold period of time. <i>See</i> 7:21-29 (“In addition to limiting ON times of switch 200d, it is desirable to limit maximum frequency</p> |

EXHIBIT B

| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|--|---|
| <p>time after transitioning the power switch to the OFF state, and wherein the primary controller is configured to refrain from setting the power switch into the ON state in response to a subsequent request signal received during the threshold period of time.</p> | <p>of these ON times. To this end, the voltage across a capacitor 226d is charged to a logic high through a resistor 225d and applied to a node Da, the D-input of flip-flop 220d. When node/Qa falls, capacitor 226d is discharged through a diode 227d, slowly to be recharged through resistor 225d. Until the capacitor 226d voltage is recharged to the D-input threshold voltage, flip-flop 220d is inhibited from turning ON switch 200d.”).</p> |
| <p>13. The power converter controller of claim 11, wherein the power converter is an isolated power converter, wherein the secondary controller is configured to be coupled to a secondary side of the power converter, and wherein the primary controller is configured to be coupled to a primary side of the power converter.</p> | <p>Fig. 4 of Morong shows a power converter (10d) that is an isolated power converter, wherein the secondary controller (elements 400d-509d) is configured to be coupled to a secondary side of the power converter (10d), and wherein the primary controller (elements 213d-242d) is configured to be coupled to a primary side of the power converter (10d).</p> |

EXHIBIT B

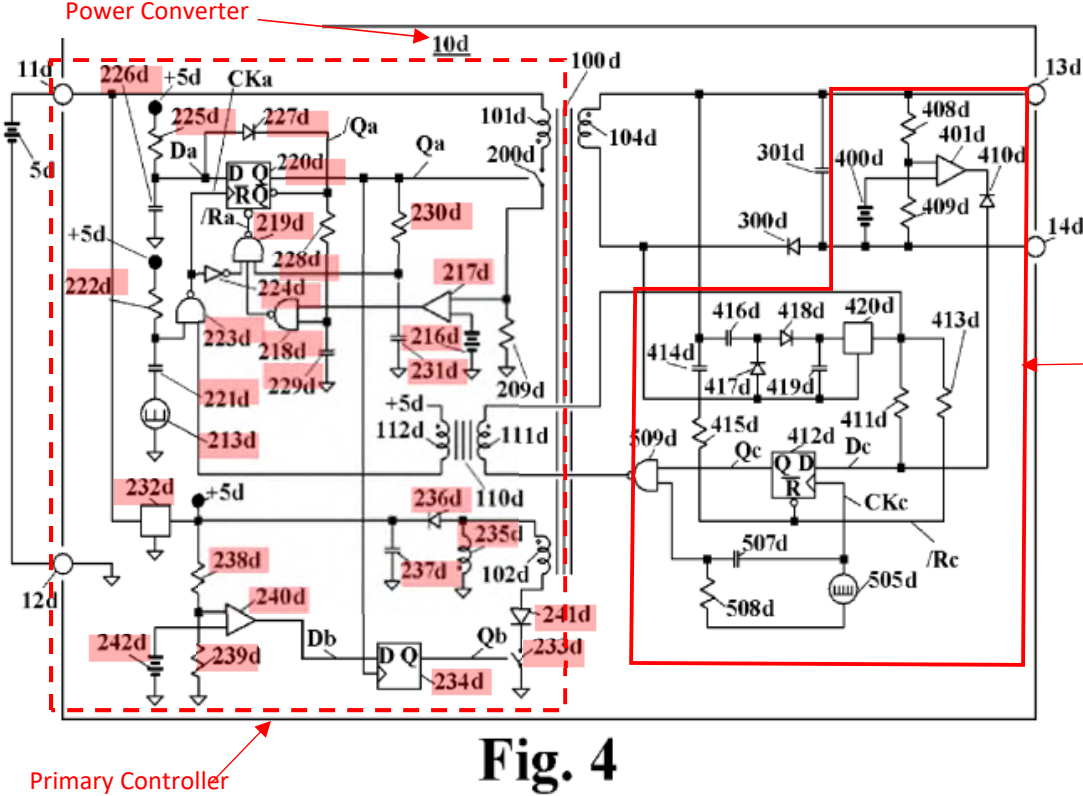
| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|---|--|
| |  <p>The diagram illustrates a power converter controller circuit. It is divided into three main functional blocks: a Primary Controller, a Power Converter, and a Secondary Controller. The Primary Controller (elements 213d-242d) receives a request signal (11d) and generates a pulse (226d) that is coupled to the Power Converter (elements 100d-200d). The Power Converter includes a transformer (101d, 104d) and a switch (200d). The Secondary Controller (elements 300d-508d) is coupled to the Power Converter and generates a pulse (400d) that is coupled to the Primary Controller. The circuit also includes various other components such as resistors (e.g., 222d, 223d, 224d, 225d, 227d, 228d, 229d, 230d, 231d, 232d, 233d, 234d, 235d, 236d, 237d, 238d, 239d, 240d, 241d, 242d), capacitors (e.g., 216d, 217d, 218d, 219d, 220d, 221d, 222d, 223d, 224d, 225d, 226d, 227d, 228d, 229d, 230d, 231d, 232d, 233d, 234d, 235d, 236d, 237d, 238d, 239d, 240d, 241d, 242d), and diodes (e.g., 213d, 214d, 215d, 216d, 217d, 218d, 219d, 220d, 221d, 222d, 223d, 224d, 225d, 226d, 227d, 228d, 229d, 230d, 231d, 232d, 233d, 234d, 235d, 236d, 237d, 238d, 239d, 240d, 241d, 242d). The circuit is powered by a 5d supply and includes a 12d input and a 13d output.</p> <p style="text-align: center;">Fig. 4</p> |
| <p>16. The power converter controller of claim 11, wherein the request signal is a pulse, and wherein the primary</p> | <p>Fig. 4 in Morong shows a power converter controller wherein the request signal is a pulse, and wherein the primary controller (elements 213d-242d) is coupled to receive the pulse (demand pulse) and set the power switch (switch 200d) into the ON state in response to the pulse. <i>See</i> 7:42-61 (“The ON pulses of switch 200d responsive to oscillator 213d are sufficiently frequent to start the converter of this embodiment, but insufficiently frequent to drive it to full output. To initiate more frequent pulses, an</p> |

EXHIBIT B

| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|---|---|
| <p>controller is coupled to receive the pulse and set the power switch into the ON state in response to the pulse.</p> | <p>oscillator 505d drives a capacitor 507d and a resistor 508d to supply differentiated pulses of about 100 nS width to a NAND gate 509d, which in turn drives a primary winding 111d of demand pulse transformer 110d, thus producing demand pulses across a secondary winding 112d thereof. These winding 112d pulses are conveyed through a NAND gate 223d to clock flip-flop 220d at up to the frequency of oscillator 505d. If all of the pulses of oscillator 505d were allowed to clock flip-flop 220d, under some conditions, the converter of this embodiment would produce excess output. To regulate this output, a flip-flop 412d is used to gate the pulses passed by NAND gate 509d. At a node CKc, oscillator 505d clocks a flip-flop 412d, which generates a logic high at a node Qc only when a logic high is present at a node Dc at the rising edge of its clock. Thus, pulses driving transformer 110d are permitted responsive to a logic high only at node Dc.”).</p> |
| <p>17. The power converter controller of claim 11, wherein the turn-off condition includes a threshold current limit, wherein the primary controller is coupled to sense an amount of current through the power switch when the power switch is in the ON state, and wherein the primary controller is coupled to transition the power switch from the ON state to the OFF state when the amount of current through the</p> | <p>Fig. 4 in Morong shows a power converter wherein the turn-off condition includes a threshold current limit, wherein the primary controller (elements 213d-242d) is coupled to sense an amount of current through the power switch (switch 200d) when the power switch is in the ON state, and wherein the primary controller is coupled to transition the power switch from the ON state to the OFF state when the amount of current through the power switch is greater than the threshold current limit. <i>See</i> 7:1-5 (“When current in resistor 209d exceeds a value set by reference 216d, comparator 217d issues a reset signal which propagates through NAND gates 218d and 219d to a node /Ra where the reset signal resets flip-flop 220d, turning OFF switch 200d.”).</p> |

EXHIBIT B

| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|--|--|
| power switch is greater than the threshold current limit. | |
| 18. The power converter controller of claim 11, wherein the turn-off condition includes a threshold amount of time, and wherein the primary controller is coupled to transition the power switch from the ON state to the OFF state when the power switch has been in the ON state for the threshold amount of time. | Fig. 4 in Morong shows a power converter controller wherein the turn-off condition includes a threshold amount of time, and wherein the primary controller (elements 213d-242d) is coupled to transition the power switch (switch 200d) from the ON state to the OFF state when the power switch has been in the ON state for the threshold amount of time. <i>See</i> 7:14-20 (“Prior to its rise, node Qa has been low, and a complementary node/Qa has been high. When node Qa rises, node/Qa falls, discharging a capacitor 229d through a resistor 228d to the threshold of NAND gate 218d in about 2 uS, and though NAND gate 219d resetting flip-flop 220d, thus limiting the maximum ON time of switch 200d, should comparator 217d fail to reset flip-flop 220d.”). |
| 20. The power converter controller of claim 11, wherein the secondary controller is coupled to transmit the request signal via a communication link, wherein the primary controller is coupled to receive the request signal via the communication | Fig. 4 in Morong shows a power converter controller wherein the secondary controller (elements 400d-509d) is coupled to transmit the request signal (demand pulse) via a communication link (demand pulse transformer 110d, wherein the primary controller (elements 213d-242d) is coupled to receive the request signal via the communication link, and wherein the communication link includes at least one of an optical communication link, a capacitive communication link, and a magnetic communication link. <i>See</i> 9:4-6 (“The converter may comprise inductive, capacitive, opto-coupled, or piezoelectric galvanic isolation circuitry to transmit demand pulses across the galvanic isolation barrier.”). |

EXHIBIT B

| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|--|---|
| link, and wherein the communication link includes at least one of an optical communication link, a capacitive communication link, and a magnetic communication link. | |
| 21. A power converter comprising: | Fig. 4 of Morong shows a power converter (10d). |
| an energy transfer element comprising a primary winding on a primary side of the power converter and a secondary winding on a secondary side of the power converter; | Fig. 4 of Morong shows a power converter comprising an energy transfer element (transformer 100d) comprising a primary winding (primary winding 101d) on a primary side of the power converter (10d) and a secondary winding (secondary winding 104d) on a secondary side of the power converter (10d). |

EXHIBIT B

| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|--|--|
| | <p style="text-align: center;">Fig. 4</p> |
| a power switch coupled to the primary winding; | Fig. 4 of Morong shows a power switch (switch 200d) coupled to the primary winding (101d). |

EXHIBIT B

| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|---|--|
| | <p style="text-align: center;">Fig. 4</p> |
| <p>a primary controller coupled to the power switch, wherein the primary controller is coupled to receive one or more request signals</p> | <p>Fig. 4 of Morong shows a primary controller (elements 213d-242d) coupled to the power switch (switch 200d), wherein the primary controller is coupled to receive one or more request signals (demand pulses) from the secondary side and transition the power switch from an OFF state to an ON state in response to each of the one or more received request signals, and wherein the primary controller is coupled to detect a turn-off condition when the power switch is in the ON state and transition the power switch from the ON state to the OFF state in response to detection of the turn-off condition. <i>See</i> 7:42-61 (“The ON pulses of</p> |

EXHIBIT B

| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|---|---|
| <p>from the secondary side and transition the power switch from an OFF state to an ON state in response to each of the one or more received request signals, and</p> | <p>switch 200d responsive to oscillator 213d are sufficiently frequent to start the converter of this embodiment, but insufficiently frequent to drive it to full output. To initiate more frequent pulses, an oscillator 505d drives a capacitor 507d and a resistor 508d to supply differentiated pulses of about 100 nS width to a NAND gate 509d, which in turn drives a primary winding 111d of demand pulse transformer 110d, thus producing demand pulses across a secondary winding 112d thereof. These winding 112d pulses are conveyed through a NAND gate 223d to clock flip-flop 220d at up to the frequency of oscillator 505d. If all of the pulses of oscillator 505d were allowed to clock flip-flop 220d, under some conditions, the converter of this embodiment would produce excess output. To regulate this output, a flip-flop 412d is used to gate the pulses passed by NAND gate 509d. At a node CKc, oscillator 505d clocks a flip-flop 412d, which generates a logic high at a node Qc only when a logic high is present at a node Dc at the rising edge of its clock. Thus, pulses driving transformer 110d are permitted responsive to a logic high only at node Dc.”).</p> |
| <p>wherein the primary controller is coupled to detect a turn-off condition when the power switch is in the ON state and transition the power switch from the ON state to the OFF state in response to detection of the turn-off condition; and</p> | <p>Fig. 4 in Morong shows a primary controller (elements 213d-242d) coupled to detect a turn-off condition when the power switch (switch 200d) is in the ON state and transition the power switch from the ON state to the OFF state in response to detection of the turn-off condition. <i>See</i> 7:1-5 (“When current in resistor 209d exceeds a value set by reference 216d, comparator 217d issues a reset signal which propagates through NAND gates 218d and 219d to a node /Ra where the reset signal resets flip-flop 220d, turning OFF switch 200d.”).</p> |
| <p>a secondary controller coupled to the secondary side and galvanically isolated from the primary</p> | <p>Fig. 4 in Morong shows a secondary controller (elements 400d-509d) coupled to the secondary side and galvanically isolated from the primary controller (elements 213d-242d), wherein the secondary controller is coupled to transmit the one or more request signals to the primary controller (<i>See</i> 6:37-39 (“FIG. 4 shows a schematic diagram of a power converter 10d, comprising a separate transformer 110d to transmit</p> |

EXHIBIT B

| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|---|--|
| <p>controller, wherein the secondary controller is coupled to transmit the one or more request signals to the primary controller, and wherein the secondary controller is coupled to control an amount of time between the transmission of each of the one or more request signals,</p> | <p>demand pulses across a galvanic isolation barrier.”)), and wherein the secondary controller is coupled to control an amount of time between the transmission of each of the one or more request signals. <i>See</i> 7:53-61 (“If all of the pulses of oscillator 505d were allowed to clock flip-flop 220d, under some conditions, the converter of this embodiment would produce excess output. To regulate this output, a flip-flop 412d is used to gate the pulses passed by NAND gate 509d. At a node CKc, oscillator 505d clocks a flip-flop 412d, which generates a logic high at a node Qc only when a logic high is present at a node Dc at the rising edge of its clock. Thus, pulses driving transformer 110d are permitted responsive to a logic high only at node Dc.”).</p> |
| <p>wherein the turn-off condition is a threshold current limit and the primary controller is coupled to adjust the threshold current limit in response to an amount of time the power switch is in the ON state.</p> | <p>Fig. 4 in Morong shows the turn-off condition is a threshold current limit (value set by reference 216d) and the primary controller is coupled to adjust the threshold current limit in response to an amount of time the power switch is in the ON state. <i>See</i> 7:1-5 (“When current in resistor 209d exceeds a value set by reference 216d, comparator 217d issues a reset signal which propagates through NAND gates 218d and 219d to a node /Ra where the reset signal resets flip-flop 220d, turning OFF switch 200d.”).</p> <p>To the extent that Power Integrations argues that Morong does not show that it adjusts the value set by reference 216d, then Djenguerian alone or in combination with Morong meets this limitation.</p> <p>Fig. 1 in Djenguerian shows a power converter (flyback power converter 100) wherein the turn-off condition is a threshold current limit and the primary controller (control circuit 115) is coupled to adjust the threshold current limit in response to an amount of time the power switch (power switch 105) is in the ON state.</p> |

EXHIBIT B

FIG. 1

As taught in Djenguerian, the turn-off condition is the power switch protective current limit threshold and the control circuit 115 is coupled to adjust the power switch protective current limit threshold in response to an amount of time the power switch 105 is in the ON state.

EXHIBIT B

| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|---|--|
| | <p>“In one example controller 115 is coupled to adjust a duty cycle of the power switch 105 to be proportional to a value of the input voltage signal multiplied by the time it takes for the current flowing in the power switch to change between two current values when the power switch is in the on state.” 4:48-53.</p> <p>“It is noted that although the above description employs the power switch switching period as the control parameter for adjustment based on the measured value of the (KVIN×t) product, more generally the ratio of the power switch on time to the power switch off time during any power switch switching cycle period, known as the power switch duty cycle, is a broader description of the same control functionality. In general, the power switch duty cycle can be adjusted by adjusting the power switch switching cycle period but also by other techniques including adjusting the power switch protective current limit threshold, directly controlling the period of time for which the power switch is on during each switching cycle period, on/off control, pulse width modulation or other suitable power converter switching techniques.” 8:22-35.</p> |
| 22. The power converter of claim 21, wherein the secondary controller includes a timing circuit that sets a minimum amount of time between the transmission of each of the request signals. | Fig. 4 in Morong shows a power converter wherein the secondary controller includes a timing circuit (at least oscillator 505d plus flip-flop 220d) that sets a minimum amount of time between the transmission of each of the request signals (demand pulses). <i>See</i> 8:50-52 (“These winding 112d pulses are conveyed through a NAND gate 223d to clock flip-flop 220d at up to the frequency of oscillator 505d.”). |
| 23. The power converter of claim 21, further comprising a communication link, wherein the secondary | Fig. 4 in Morong shows a power converter comprising a communication link (demand pulse transformer 110d), wherein the secondary controller (elements 400d-509d) is coupled to transmit the one or more request signals (demand pulses) via the communication link, wherein the primary controller (elements 213d-242d) is coupled to receive the one or more request signals via the communication link, and wherein the communication link includes at least one of an optical communication link, a capacitive |

EXHIBIT B

| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|--|---|
| <p>controller is coupled to transmit the one or more request signals via the communication link, wherein the primary controller is coupled to receive the one or more request signals via the communication link, and wherein the communication link includes at least one of an optical communication link, a capacitive communication link, and a magnetic communication link.</p> | <p>communication link, and a magnetic communication link. <i>See</i> 9:4-6 (“The converter may comprise inductive, capacitive, opto-coupled, or piezoelectric galvanic isolation circuitry to transmit demand pulses across the galvanic isolation barrier.”).</p> |
| <p>25. The power converter of claim 22, wherein the timing circuit is coupled to operate in a first state until triggered to operate in a second state, wherein the timing circuit is in the second state for a holding period and transitions back to the first state at an end of the holding</p> | <p>Fig. 4 in Morong shows a power converter wherein the timing circuit (at least oscillator 505d plus flip-flop 412d) is coupled to operate in a first state (rising edge of clock signal at node CKc from oscillator 505d) until triggered to operate in a second state (duration between consecutive rising edges of clock signal at node CKc from oscillator 505d), wherein the timing circuit is in the second state for a holding period and transitions back to the first state at an end of the holding period, and wherein the holding period sets a minimum amount of time between the transmission of two consecutive request signals. <i>See</i> 7:42-61 (“The ON pulses of switch 200d responsive to oscillator 213d are sufficiently frequent to start the converter of this embodiment, but insufficiently frequent to drive it to full output. To initiate more frequent pulses, an oscillator 505d drives a capacitor 507d and a resistor 508d to supply differentiated pulses of about 100 nS width to a NAND gate 509d, which in turn drives a primary winding 111d of demand pulse transformer 110d, thus producing demand pulses across a secondary winding 112d thereof.</p> |

EXHIBIT B

| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|--|--|
| <p>period, and wherein the holding period sets a minimum amount of time between the transmission of two consecutive request signals.</p> | <p>These winding 112d pulses are conveyed through a NAND gate 223d to clock flip-flop 220d at up to the frequency of oscillator 505d. If all of the pulses of oscillator 505d were allowed to clock flip-flop 220d, under some conditions, the converter of this embodiment would produce excess output. To regulate this output, a flip-flop 412d is used to gate the pulses passed by NAND gate 509d. At a node CKc, oscillator 505d clocks a flip-flop 412d, which generates a logic high at a node Qc only when a logic high is present at a node Dc at the rising edge of its clock. Thus, pulses driving transformer 110d are permitted responsive to a logic high only at node Dc.”)</p> |
| <p>26. The power converter of claim 25, wherein the secondary controller includes a secondary switch control circuit coupled to sense an output quantity of the power converter and transmit one of the request signals to the primary controller when the sensed output quantity is less than a desired output quantity and the timing circuit is in the first state, and wherein the secondary switch control circuit triggers the timing circuit in response to</p> | <p>Fig. 4 in Morong shows a power converter wherein the secondary controller (elements 400d-509d) includes a secondary switch control circuit (comparator 401d) coupled to sense an output quantity (voltage at terminals 13d and 14d) of the power converter and transmit one of the request signals to the primary controller when the sensed output quantity is less than a desired output quantity (proportional to voltage of reference 400d) and the timing circuit (at least oscillator 505d plus flip-flop 412d) is in the first state (rising edge of clock signal at node CKc from oscillator 505d), and wherein the secondary switch control circuit triggers the timing circuit in response to transmitting the one or more request signal (demand pulse). <i>See</i> 8:6-19 (“Node Dc is usually held at a logic high by a resistor 411d, thus enabling pulses gated by flip-flop 412d. However, between terminals 13d and 14d is disposed a voltage divider comprising resistors 408d and 409d, the voltage at the junction of which is applied to an input of a comparator 401d. Should the voltage at that junction exceed the voltage of a reference 400d, also applied to a comparator 401d input, an output of comparator 401d will drop to a logic low, drawing current through a diode 410d, thus presenting a logic low at node Dc and, after clocking, responsively at node Qc, inhibiting pulses through gate 509d that would otherwise turn ON switch 200d. Thus, the voltage between terminals 13d and 14d is regulated responsive to the voltage of reference 400d.”). To the extent that Power Integrations argues that Fig. 4 of Morong does not expressly show a secondary switch control circuit that triggers the timing circuit in response to transmitting the request signal, it would have be obvious to a person of ordinary skill in the art to implement a power converter having this feature based on the teachings in at least Morong and Djenguerian.</p> |

EXHIBIT B

| U.S. Pat. No. 9,166,486 | U.S. Pat. No. 9,071,152 (Morong) + U.S. Pat. No. 7,746,050 (Djenguerian) |
|--|---|
| transmitting the one or more request signal. | |